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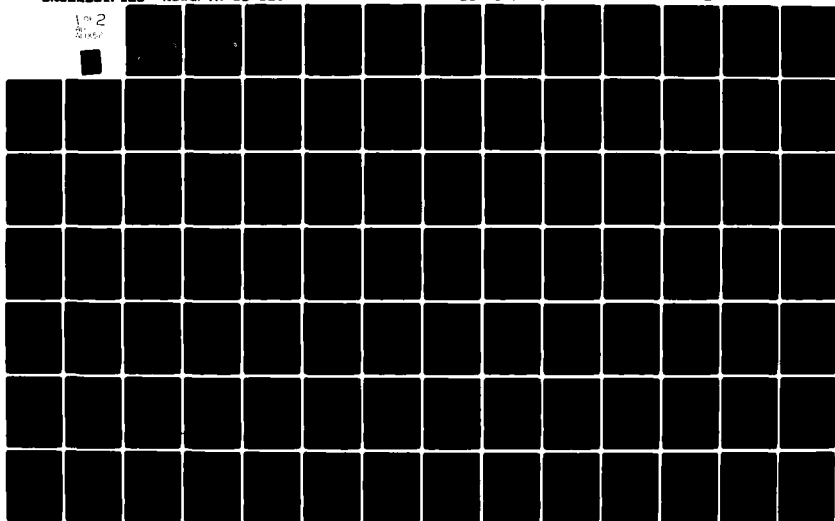
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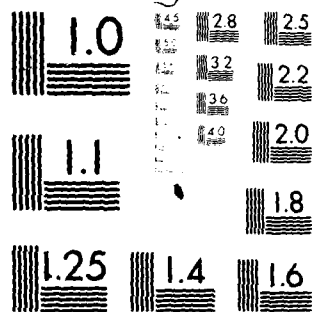
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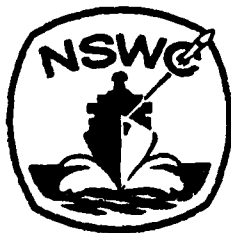
BY ROBERT H. DAVIS DOROTHY M. GREATHOUSE

UNDERWATER SYSTEMS DEPARTMENT

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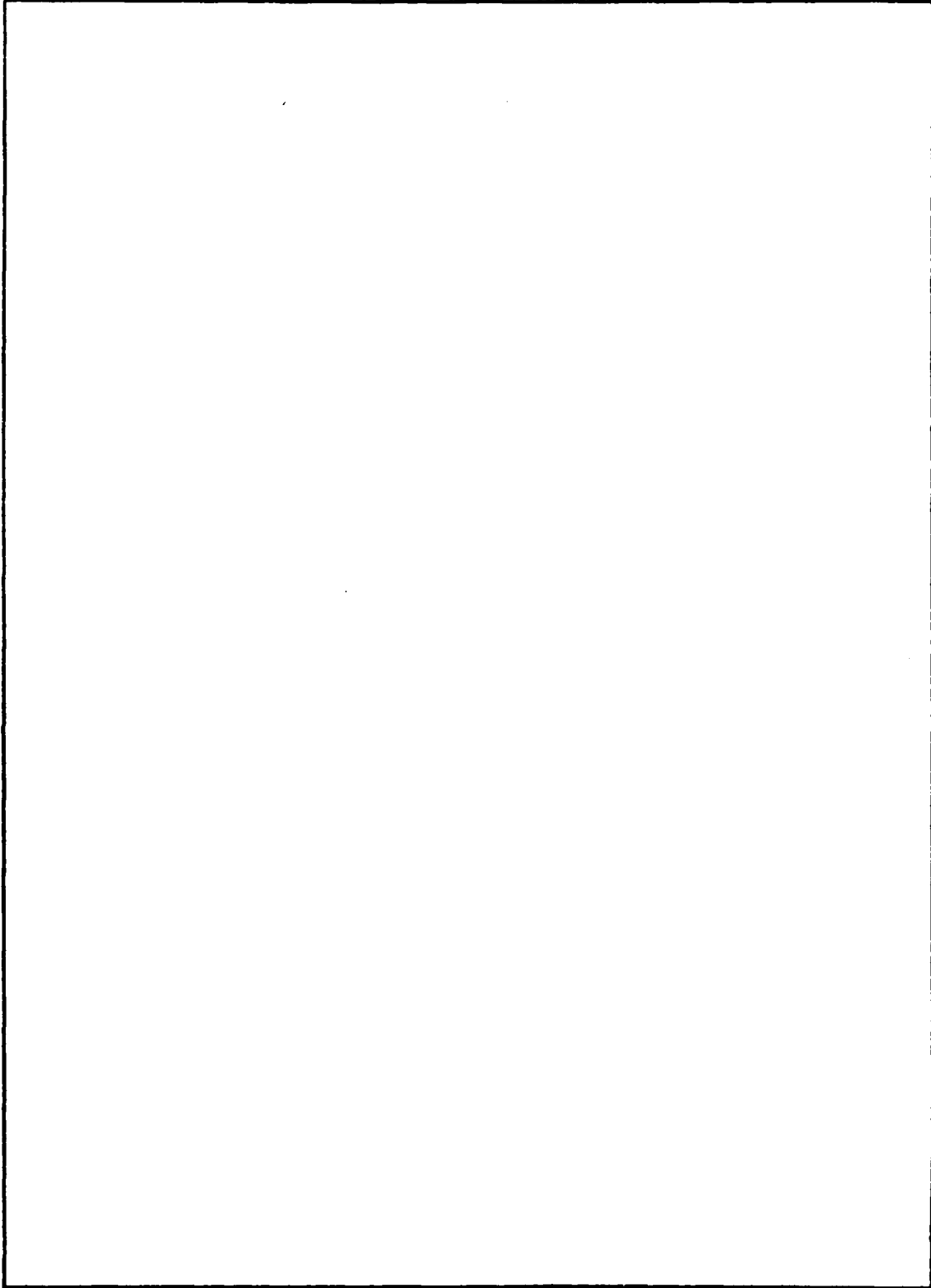
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FOREWORD

This report describes the Arithmetic Processor (AP) microprograms (or MACROS) developed for the passive synthesis portion of the Digital Acoustic Sensor Simulator (DASS) program. These microprograms are written for the Arithmetic Processor of the AN/UYS-1 Advanced Signal Processor (ASP) built by IBM, Inc. Approximately half of these programs are highly specialized for the DASS application and are of limited general use. The others have more general application and should be of interest to other ASP users.

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CONTENTS

<u>Chapter</u>		<u>Page</u>
1	INTRODUCTION	1-1
2	BROADBAND AMPLITUDE (BBAMP) MACRO	2-1
3	DISCRETE LINE SPECTRA GENERATION (DSCLN) MACRO	3-1
4	SINGLE REAL FFT (SRFFT) MACRO	4-1
5	SCALE AND ADD TWO ARRAYS (SCLA2) MACRO	5-1
6	ASYNCHRONOUS SAMPLE, SCALE AND SUM (ASSSS) MACRO	6-1
7	SCALE AND ADD THREE ARRAYS (SCLA3) MACRO	7-1
8	FILTER TWO AND SUM THREE ARRAYS (F22S3) MACRO	8-1
9	DEMODULATED NOISE (DEMON) MACRO	9-1
APPENDIX A	AP MICROPROGRAM SOURCE LISTINGS	A-1

ILLUSTRATIONS

<u>Figure</u>		<u>Page</u>
3-1	CONSTRUCTION OF HANNING APPROXIMATION	3-2
3-2	DSCLN ILLUSTRATION OF TERMINOLOGY	3-3
3-3	COMPARISON OF APPROXIMATION AND EXACT HANNING FUNCTION	3-5
6-1	ASSSS INPHASE MAIN LOOP FLOW	6-4
6-2	ASSSS OUTPHASE MAIN LOOP FLOW	6-5

TABLES

<u>Table</u>		<u>Page</u>
2-1	BBAMP AP MICROPROGRAM SCALING	2-5
2-2	BBAMP AEC REGISTER MAP.	2-6
2-3	BBAMP AE REGISTER MAP	2-7
2-4	BBAMP/DSCLN WORKING STORE MAP	2-8
2-5	BBAMP PROGRAM CODING CHART.	2-9
3-1	DSCLN AP MICROPROGRAM SCALING	3-10
3-2	DSCLN AEC REGISTER MAP.	3-13
3-3	DSCLN AE REGISTER MAP	3-14
3-4	DSCLN PROGRAM CODING CHART.	3-15
4-1	SRFFT AP MICROPROGRAM SCALING	4-5
4-2	SRFFT AEC REGISTER MAP.	4-6
4-3	SRFFT AE REGISTER MAP	4-7
4-4	SRFFT WORKING STORE MAP	4-8
4-5	SRFFT PROGRAM CODING CHART.	4-9
5-1	SCLA2 AP MICROPROGRAM SCALING	5-4
5-2	SCLA2 AEC REGISTER MAP.	5-5
5-3	SCLA2 AE REGISTER MAP	5-6
5-4	SCLA2 WORKING STORE MAP	5-7
5-5	SCLA2 PROGRAM CODING CHART.	5-8
6-1	ASSSS AP MICROPROGRAM SCALING	6-11
6-2	ASSSS AEC REGISTER MAP	6-12
6-3	ASSSS AE REGISTER MAP	6-13
6-4	ASSSS WORKING STORE MAP	6-14
6-5	ASSSS PROGRAM CODING CHART.	6-15
7-1	SCLA3 AP MICROPROGRAM SCALING	7-4
7-2	SCLA3 AEC REGISTER MAP.	7-5

TABLES (Cont.)

<u>Table</u>		<u>Page</u>
7-3	SCLA3 AE REGISTER MAP	7-6
7-4	SCLA3 WORKING STORE MAP	7-7
7-5	SCLA3 PROGRAM CODING CHART.	7-8
8-1	F22S3 AP MICROPROGRAM SCALING	8-4
8-2	F22S3 AEC REGISTER MAP.	8-5
8-3	F22S3 AE REGISTER MAP	8-6
8-4	F22S3 WORKING STORE MAP	8-7
8-5	F22S3 PROGRAM CODING CHART.	8-8
9-1	DEMON AP MICROPROGRAM SCALING	9-5
9-2	DEMON AEC REGISTER MAP.	9-6
9-3	DEMON AE REGISTER MAP	9-7
9-4	DEMON WORKING STORE MAP	9-8
9-5	DEMON PROGRAM CODING CHART.	9-9

CHAPTER 1
INTRODUCTION

This report describes the Arithmetic Processor (AP) microprograms (or MACROS) developed for the passive synthesis portion of the Digital Acoustic Sensor Simulator (DASS) program. These microprograms are written for the Arithmetic Processor of the AN/UYS-1 Advanced Signal Processor (ASP) built by IBM, Inc. Approximately half of these programs are highly specialized for the DASS application and are of limited general use. The others have more general application and should be of interest to other ASP users. A brief description of each MACRO is given below. A complete description of each MACRO is provided in its corresponding chapter. Chapter format, for the most part, conforms to a previous IBM publication.¹ Each chapter contains a functional description of the algorithm implemented by the microprogram, a mathematical description giving the exact computations performed by the microcode, a description of the microcode implementation from the viewpoint of sequencing and control, and tabulation of register usage and program statistics. In addition, each chapter contains detailed charts for:

- a) Program coding and timing
- b) Arithmetic Element Controller (AEC) and Arithmetic Element (AE) register assignments
- c) Working Store (WS) layout of input and output data
- d) Scaling analysis of input, intermediate and output data.

The program coding charts are a fixed-format representation of the sequence of micro-instructions for each microprogram. Each line on the chart represents the events occurring during one 100 ns microstep. The register assignment charts list the computational elements which are stored in each AE register during microprogram execution. The Working Store layouts illustrate the WS data organization used in DASS, although other equivalent layouts could be used. The scaling analysis

¹Proteus AU Microprogram Design Document, Code Ident 6259764, IBM, Inc., 01 Aug 1976.

charts list each partial result of the computations and give its fixed-point scaling in terms of the assumed position of the binary point. An Fx scaling indicates that the partial result is a 32-bit (fullword) number with the binary point x bits to the left ($x > 0$) or right ($x < 0$) of the midpoint of the word (16 bits from either end). An Hx scaling indicates a 16-bit (halfword) number with an assumed binary point x bits to the left ($x > 0$) or right ($x < 0$) of the right end of the halfword.

Appendix A contains the source listings for each microprogram.

BBAMP (BROADBAND AMPLITUDE)

BBAMP weights an array of complex spectral components by a set of spectral amplitudes and convolves the result with the spectrum of a sine pulse. This MACRO is peculiar to DASS and has limited application to other problems.

DSCLN (DISCRETE LINE SPECTRA GENERATION)

DSCLN generates the appropriate spectral components for discrete line components of arbitrary frequency, amplitude and phase and adds these spectral components to the Broadband spectrum generated by BBAMP. This MACRO is also peculiar to DASS and has limited application to other problems.

SRFFT (SINGLE REAL FFT)

SRFFT performs the additional pass or operation necessary, in addition to the basic (complex to complex) FFT algorithm, to effect transforms between real (time) arrays and single sided complex (frequency) arrays. This MACRO should be of general interest and applicability.

SCLA2 (SCALE AND ADD TWO ARRAYS)

SCLA2 provides the combination of two arrays, X and Y, to produce an output array Z. Provision is made for independent scaling of each of the two input arrays. This MACRO is of general applicability.

ASSSS (ASYNCHRONOUS SAMPLE, SCALE AND SUM)

ASSSS resamples an input array at a rate which is non-integrally related to the origin sample rate. Linear interpolation is performed to reduce aliasing. Resampled data is then scaled and added to a second array. This MACRO is of some, but not extensive, general usefulness.

SCLA3 (SCALE AND ADD THREE ARRAYS)

SCLA3 provides the combination of three arrays X, Y, and Z to produce an output array W. Provision is made for independent scaling of each of the three input arrays. The MACRO is of general applicability.

F22S3 (FILTER TWO AND SUM THREE ARRAYS)

F22S3 is intended for filtering each of two inputs and adding the sum of the filter outputs to a third input. Each of the two filters is a two-pole recursive filter with independent parameters. This MACRO may be of use in other applications.

DEMON (DEMODULATED NOISE)

DEMON is used to generate two signal components, each consisting of a broadband signal modulated by a periodic signal. The MACRO additionally combines the two components with a third input to produce a composite output signal. This MACRO is of some, but not extensive, general usefulness.

CHAPTER 2

BROADBAND AMPLITUDE (BBAMP) MACRO

INTRODUCTION

The Broadband spectra generation algorithm is described in detail in a previous publication.² Briefly, the broadband spectra is described by an array A of 860 numbers representing the spectral amplitude at 860 frequencies evenly spaced across the band of interest. The 860 frequencies are given by:

$$f_n = f_c \left(n - \frac{1}{2} \right); n = 1, 2, \dots, 860$$

where f_c is the DFT cell width. Each specific spectral array B is generated by the following algorithm:

$$BR_i = \frac{1}{2} (A_i RR_i - A_{i+1} RR_{i+1})$$

$$BI_i = \frac{1}{2} (A_i RI_i - A_{i+1} RI_{i+1})$$

$$BR_0 = BI_0 = 0$$

$$A_{860} \text{ must be } 0$$

$$BR_i = BI_i = 0 \text{ for } i \text{ greater than } 860$$

where BR_i and BI_i are the real and imaginary components of the i th cell of the output spectral array B, $i=0$ to 1023, and RR_i and RI_i are independent samples from a Gaussian random process with zero mean and variance of $\frac{1}{2}$.

The DFT (single sided complex to real) of the B array produces a 2048 sample time waveform segment with a sine pulse weighting. Successive segments generated in this manner are overlapped by 1024 samples and combined to form the output broadband time waveform. Since the segments are uncorrelated (all RR 's, RI 's are independent) the overlapped segments add incoherently to yield a random function having the desired average spectral behavior and stationary first order

²DAVIS, R. H., "Synthesis of Steady-State Signal Components by an All-Digital System", NOLTR 74-215, Naval Ordnance Laboratory, (Now Naval Surface Weapons Center) 05 Dec 1974.

statistics.

FUNCTIONAL DESCRIPTION

BBAMP MACRO consists of four steps to obtain the non-zero broadband spectrum. The first step is to generate a "variator" factor which is a continuous, piecewise linear function defined over the non-zero amplitudes. This function is produced by beginning at each breakpoint with the value of the function and adding an increment (signed) for each successive value until the next breakpoint is reached. The second step is to multiply the AMP element by the variator value generated as described above to produce the amplitude for that spectral cell. This amplitude is then used in the third step to scale the two components of the corresponding RN (Random Number) array element to produce the "half cell" frequency components. The final step is to form the output array element by linearly combining the i^{th} half cell components with the previous $((i-1)^{\text{st}})$ half cell components.

MATHEMATICAL DESCRIPTION

$$\text{Phase 1: } \text{CAV}_i = \text{CAV}_{i-1} + \text{DAV}_j$$

where CAV_{i-1} is the variator function value at the last cell and DAV_j is the increment value for the (current) j^{th} linear segment. If i corresponds to the $j+1^{\text{st}}$ breakpoint,

$$\text{CAV}_i = \text{AV}_{j+1}$$

where AV is the initial value for the $j+1$ segment obtained from the VAR buffer.

$$\text{Phase 2: } \text{VA}_i = \text{CAV}_i * \text{A}_i$$

where A_i is the AMP value for the i^{th} cell, and VA_i is the variated amplitude.

$$\text{Phase 3: } \text{BHR}_i = \text{VA}_i * \text{RR}_i$$

$$\text{BHI}_i = \text{VA}_i * \text{RI}_i$$

where RR_i and RI_i are the real and imaginary values, respectively, of the i^{th} RN element, and BHR_i and BHI_i are the properly scaled components for the "half-cell" frequencies.

$$\text{Phase 4: } \text{BR}_i = \text{BHR}_i - \text{BHR}_{i-1}$$

$$\text{BI}_i = \text{BHI}_i - \text{BHI}_{i-1}$$

where BR_i and BI_i are the final output components of the i^{th} element of the BB array.

IMPLEMENTATION

BBAMP is implemented with a ten-instruction main loop which processes one

pair of A's (amplitudes), R's (complex random numbers) and B's (output broadband spectral cells). An eighteen-instruction preamble loads the pipe such that two valid B's are produced on each pass through the main loop. An eight-instruction segment of code contained within the main loop is skipped except when a new set of variator parameters is required for a new linear segment. The variator array is stored as two 32-bit word pairs - the first word contains the initial variator value for the i^{th} corresponding linear segment in the high order 16 bits, and a count parameter determining the number of pairs of amplitudes for which the segment is to apply in the low order 16 bits. The second word contains the increment value for the segment. The count parameter is interpreted as the number of amplitude pairs - 1, and thus a count of zero produces a segment of length 2. The first count parameter is interpreted by the preamble as number of pairs - 2; and therefore, the minimum length of the first segment is 4. The count is tested for zero and decremented each pass through the main loop. The embedded variator function change code is executed if the zero test is met.

The inside loop is controlled by BNZ8. An outside loop controlled by BNZ9 allows arrays of greater than 512 points to be processed. BBAMP is intended to be combined with DSCLN in a SUPER MACRO, and returns to the SUPER MACRO Code via BR4 upon completion.

SCALING

See Table 2-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 2-2.

ADDRESS REGISTERS

- ARO - The increment code is initialized to 1. The address portion is initialized to the address of the AMP buffer.
- AR1 - The increment code is initialized to 1. The address portion is initialized to the address of the VAR buffer.
- AR2 - The increment code is initialized to 1. The address portion is initialized to the address of the RN buffer.
- AR3 - The increment code is initialized to 1. The address portion is initialized to the address of the output BB buffer. An initial dummy read with a "subtract increment" directive effectively initializes the address portion to BB-1.

INCREMENT REGISTERS

INC 0, 1, 2, 3 - Wrap code must be 1024.

BRANCH REGISTERS

- BR4 - Unconditional branch to return to SUPER MACRO at completion of BBAMP. If BBAMP and DSCLN are not combined by a SUPER MACRO, BR4 should branch to STOP.
- BCRO - Conditional branch over the variator change portion of the main loop. Conditioned on the sign of the incremented count CT.
- BNZ8 - Branch register controlling the number of times the inner loop is executed.
- BNZ9 - Branch register controlling the number of times the outer loop is executed. Total number of data pairs processed is product of inner times outer loop executions. BNZ9 allows processing of arrays longer than 512 points.

SINE/COSINE DESTINATION REGISTERS

Not applicable.

DECIMATE REGISTER

Not applicable.

SCALE FACTOR REGISTERS

- SFOH - All True/Direct.
- SFOL - Left, center, and right prescalers - True/Direct, postscaler - True/Left 4.

ARITHMETIC ELEMENT REGISTER MAP

See Table 2-3.

WORKING STORE MAP

See Table 2-4.

PROGRAM CODING CHART

See Table 2-5.

TABLE 2-1 BBAMP AP MICROPROGRAM SCALING

[illegible]

TABLE 2-2 BBAMP AEC REGISTER MAP

Incr Code		Address Register				WS Wrap		Increment Register				Memory Address Register			
0	3	4			15	0	3	4			15				
0	1	A(AMP)				0					BBAMP				
1	1	A(VF)				0									
2	1	A(RN)				0					Sin/Cos Destination Register				
3	1	A(BB)				0					AE0 AE1 AE2 AE3				
											0				
											1				
											2				
											3				
4											Decimate Register				
5											Count Reset				
6															
7											Comments				
N = number of spectral cells to process.															

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers

Branch Address		Count Reset Spare Branch Address			
0	15	0	78	1516 21 22	31
0	BB2	8	$\frac{N}{4} - 1$	$\frac{N}{4} - 1$	BB1
1		9	1	1	BB1
2		A			
3		B			
4	STOP	C			
5		D			
6		E			
7		F			

Comments

N = number of spectral
cells to process.

TABLE 2-3 BBAMP AE REGISTER MAP

MLR				MRR			
0H	M1, CAV1	CAV2	0L	0H	M1, A1	A2	0L
1H	VA1	VA2	1L	1H	RR1	RI1	1L
2H	AV1	CT1	2L	2H	RR2	RI2	2L
3H	DUMMY	READ	3L	3H			3L

ALIR				ACIR			
0H	BH R1		0L	0H	P1, BH#2		0L
1H	BH I1		1L	1H	BH#2		1L
2H	AV	CT	2L	2H			2L
3H	D V		3L	3H			3L

ARIR				AEOR			
0	TEMP			0H			0L
1				1H	BR1	BI1	1L
2				2H	BR2	BI2	2L
3				3H			3L

SCALE FACTOR REGISTERS							
AE0				AE1			
0H	0	0	0	0	0	0	0
1H							
2H							
3H							

ALOR				ACOR				AROR			
0				0	CAV			0	DAV		
1				1	CT			1	P1		
2				2				2			
3				3				3			

TABLE 2-4 BBAMP/DSCLN WORKING STORE MAP

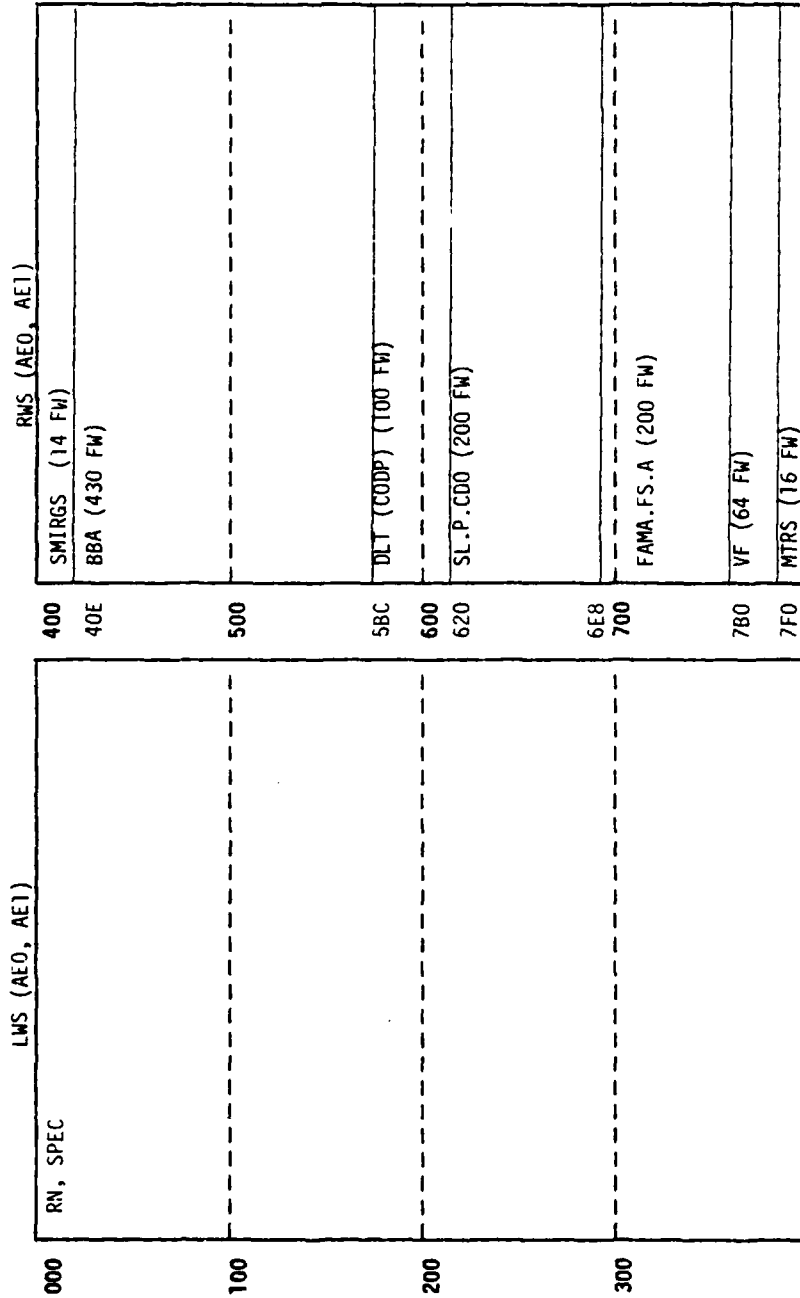


TABLE 2-5 BBAMP PROGRAM CODING CHART

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TABLE 2-5 (CONTINUED)

[illegible]

TABLE 2-5 (CONTINUED)

[illegible]

CHAPTER 3

DISCRETE LINE SPECTRA GENERATION (DSCLN) MACRO

INTRODUCTION

The discrete line spectra generation algorithm is described in detail in a previous publication.³ Briefly, for each discrete line to be added to the spectrum of each 2048 sample time waveform generated, complex components are added to six frequency cells - three on each side of the desired frequency. The magnitudes and phases of the six complex components are computed from the desired frequency and amplitude for the segment to be generated and from the frequency and phase of the preceding segment.

The exact amplitude weighting for the six components is given by the periodic Hanning function.⁴ For DSCLN MACRO, a three-segment approximation is used based on sine and cosine functions derived from the fractional part of the desired frequency. Figure 3-1 illustrates the use of quarter-cycle and half-cycle trig functions to generate the desired weighting function. In Figure 3-2, for a desired spectral line of amplitude A at C + D (C, the next lower cell index and D, the fractional distance to the specified line position) the following computations are performed to obtain the magnitudes for the six cell components.

For cell c - 2:

$$\begin{aligned} M_{c-2} &= A(.035*\sin(\pi D)*\cos(\frac{\pi D}{2})) \\ &= A(.07*\sin(\frac{\pi D}{2})*\cos^2(\frac{\pi D}{2})) \end{aligned}$$

For cell c - 1:

$$\begin{aligned} M_{c-1} &= A(.5 - .5*\sin(\frac{\pi D}{2}) + .026*\sin(\pi D)) \\ &= A(.5 - .5*\sin(\frac{\pi D}{2}) + .052*\sin(\frac{\pi D}{2})*\cos(\frac{\pi D}{2})) \end{aligned}$$

³DAVIS, R. H., "Synthesis of Steady-State Signal Components by an All-Digital System", NOLTR 74-215, Naval Ordnance Laboratory (now Naval Surface Weapons Center), 05 Dec 1974.

⁴Ibid.

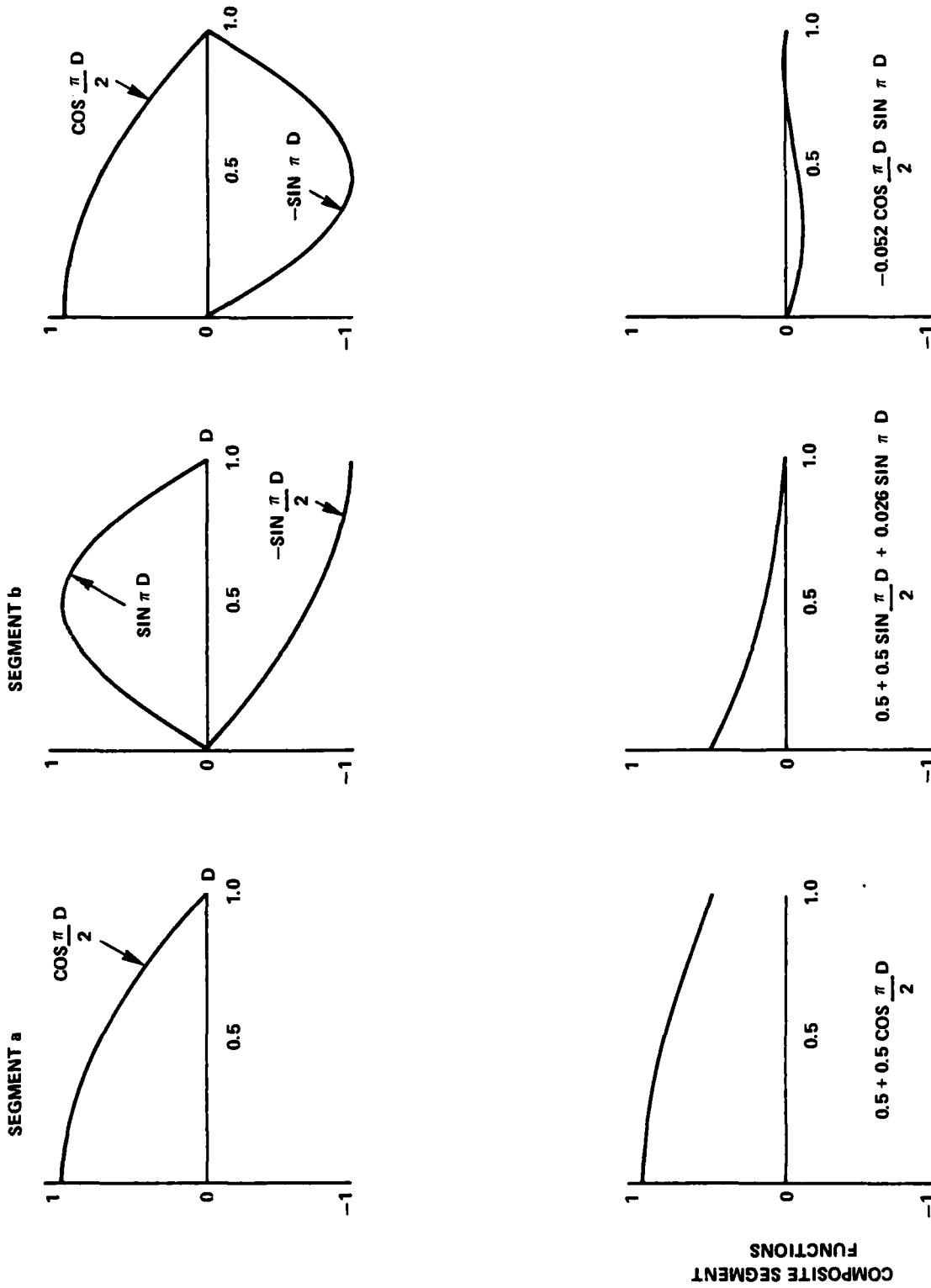


FIGURE 3-1 CONSTRUCTION OF HANNING APPROXIMATION

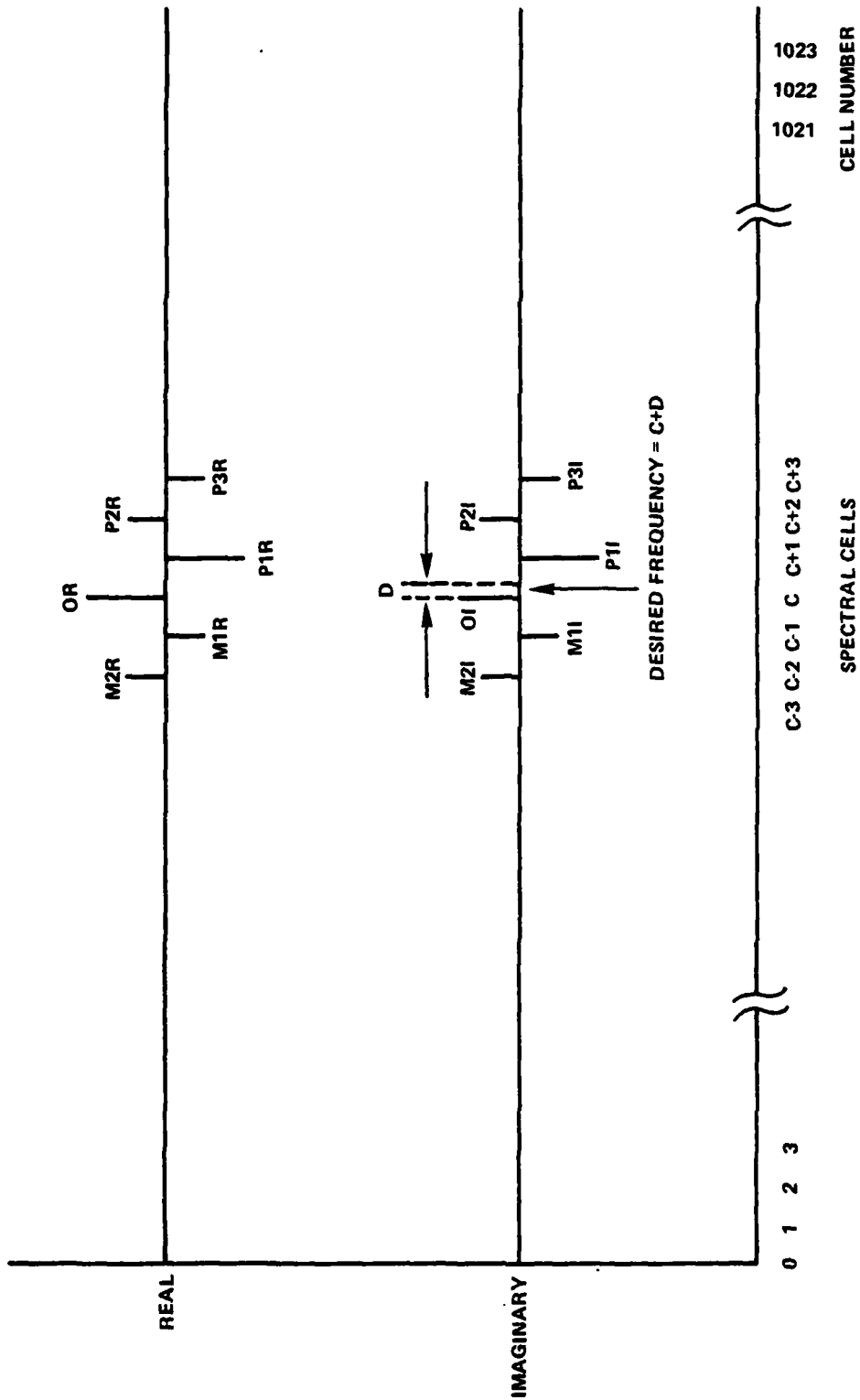


FIGURE 3-2 DSCLN ILLUSTRATION OF TERMINOLOGY

For cell c:

$$M_c = A(.5 + .5 \cos(\frac{\pi D}{2}))$$

For cell c + 1:

$$M_{c+1} = A(.5 + .5 \sin(\frac{\pi D}{2}))$$

For cell c + 2:

$$M_{c+2} = A(.5 - .5 \cos(\frac{\pi D}{2}) + .052 \sin(\frac{\pi D}{2}) \cos(\frac{\pi D}{2}))$$

And for cell c + 3:

$$\begin{aligned} M_{c+3} &= A(.035 \sin(\pi D) \cos(\frac{\pi D}{2})) \\ &= A(.07 (\sin^2(\frac{\pi D}{2}) \cos(\frac{\pi D}{2}))). \end{aligned}$$

Given D, the $\sin(\frac{\pi D}{2})$ and $\cos(\frac{\pi D}{2})$ are computed and combined to form the above functions. For a desired phase P, the component phases are set to -P, -P, P, -P, P, P.

Figure 3-3 is a BASIC generated plot comparing the three-segment approximation to the exact Hanning Function.

FUNCTIONAL DESCRIPTION

DSCLN MACRO consists of two phases of computation for each discrete line. The first phase computes the center frequency, adds the FM perturbation to obtain the instantaneous frequency, and computes the initial phase to be used for the next iteration of DSCLN. The first phase also computes the modulated amplitude to be used during the second phase computations of the current iteration. The second phase computes the six complex spectral components for each line based on the instantaneous frequency and phase stored in the Discrete Line Table (DLT) input data on the amplitude just obtained during Phase 1. The six components are then added to the appropriate cells of the spectrum being constructed.

MATHEMATICAL DESCRIPTION

For the i^{th} line during the j^{th} iteration, the following computations are performed:

Phase 1: $CDO_{i, j+2} = CDO_{i, j+1} + SL_i$

where $CDO_{i, j}$ is the center frequency for the j^{th} iteration and SL_i is the slew rate for the i^{th} line. Note that this computation produces the center frequency CDO_i valid for the second following iteration

$$FSM_{i, j+1} = FS_i * FM_{i, j+1}$$

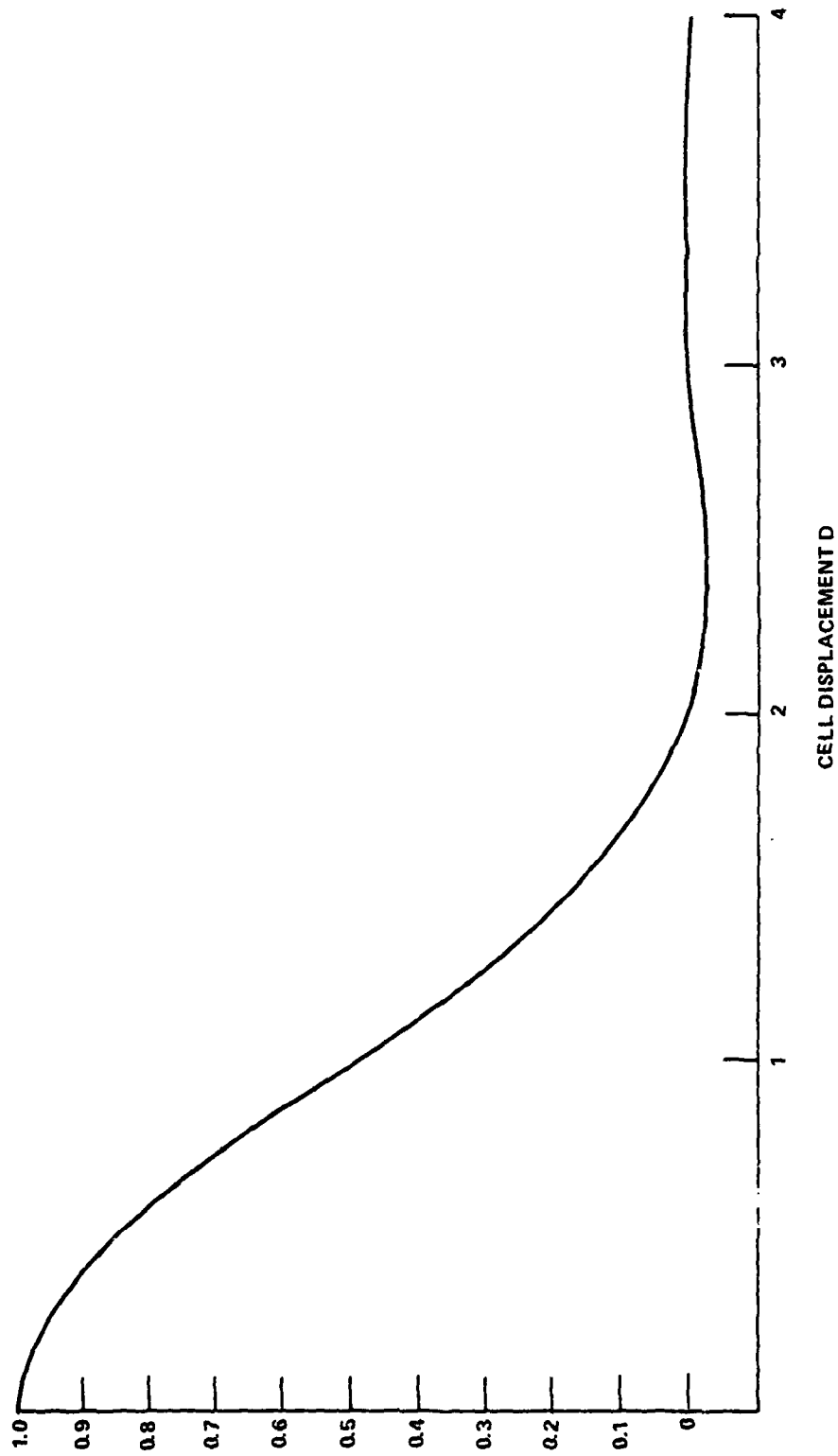


FIGURE 3-3 COMPARISON OF APPROXIMATION AND EXACT HANNING FUNCTION

where $FSM_{i,j+1}$ is the appropriately scaled FM perturbation for the i^{th} line during the $(j+1)^{st}$ iteration.

$$P_{i,j+1} = LO(P_{i,j} + \frac{3}{4}CD_{i,j} - \frac{1}{4}CD_{i,j+1})$$

where $CD_{i,j}$ is the instantaneous frequency for the j^{th} iteration.

$$A_{i,j} = A_i * AM_{i,j}$$

where A_i is the unmodulated line amplitude for the i^{th} line, and $AM_{i,j}$ is the amplitude modulation factor for the i^{th} line during the j^{th} iteration.

$$CODP_{i,j+1} = [CDO_{i,j+1} + FSM_{i,j+1}]$$

Integer part plus fraction part divided by 4 - where the integer part (H.O. 16 bits) is the center cell number C and the fractional part (L.O. 16 bits) is used as an angle argument ϕD (in BAM) in computing the Hanning coefficients.

Phase 2:

Let $A = A_{i,j}$

$$K = \cos(2\pi * P)$$

$$Z = \sin(2\pi * P)$$

$$C = \cos(2\pi * \phi D)$$

$$S = \sin(2\pi * \phi D)$$

$$7 = .07$$

$$5 = .052$$

BM2 (R,I) = Initial contents of cell C-2

BM1 (R,I) = Initial contents of cell C-1

B0 (R,I) = Initial contents of cell C

BP1 (R,I) = Initial contents of cell C+1

BP2 (R,I) = Initial contents of cell C+2

BP3 (R,I) = Initial contents of cell C+3

M2 (R,I) = Modified contents of cell C-2

M1 (R,I) = Modified contents of cell C-1

B (R,I) = Modified contents of cell C

P1 (R,I) = Modified contents of cell C+1

P2 (R,I) = Modified contents of cell C+2

P3 (R,I) = Modified contents of cell C+3

The following computations are performed:

$$M2R = BM2R - 7CCSAK$$

$$M2I = BM2I - 7CCSAZ$$

$M1R = BM1R + 1/2(ASK-AK) - 5SCAK$
 $M1I = BM1I + 1/2(ASZ-AZ) - 5SCAZ$
 $OR = BOR + 1/2(AK+ACK)$
 $OI = BOI + 1/2(AZ+ACZ)$
 $PIR = BP1R - 1/2(AK+ASK)$
 $P1I = BP1I - 1/2(AZ+ASZ)$
 $P2R = BP2R + 1/2(ACK-AK) + 5SCAK$
 $P2I = BP2I + 1/2(ACZ-AZ) + 5SCAZ$
 $P3R = BP3R + 7CSSAK$
 $P3I = BP3I + 7CSSAZ$

IMPLEMENTATION

DSCLN is implemented with a 48-instruction main loop which processes one set of Minor Frame (MNF) computations for one line. An eighteen-instruction preamble generates the parameters 7 and 5 and two auxiliaries, M1 and P1, used in the main loop, and initializes the pipe for the computations for the first line. The loop count is controlled by BNZ.A, which should be set to the number of lines to be processed minus one. Since DSCLN is the last AP program to be executed under the SUPER MACRO, SM1, a halt is executed after completion.

Since intermediate results CDO, CDDP and P are updated in Working Store by DSCLN, this area of WS must be returned to Bulk Store upon completion of DSCLN.

SCALING

See Table 3-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 3-2.

ADDRESS REGISTERS

- ARO - The initial value is set to $\cos^{-1}(7) = 27C8$. During main loop computations ARO contains the spectral cell addresses C-2, ..., C+3.
- AR1 - The initial value is set to $\sin^{-1}(5) = 2809$. During main loop computations AR1 contains the fraction ϕD from which the coefficients C and S are obtained.
- AR2 - During main loop computations AR2 is loaded with FMA and used to access the MTR functions for FM values.

NSWC TR 81-313

- AR3 - During main loop computations AR3 is loaded with AMA and used to access the MTR functions for AM values.
- AR4 - The increment code is initialized to 1. The address portion is initialized to the starting address of the SLP, CDO data area.
- AR5 - The increment code is initialized to 1. The address portion is initialized to the starting address of the FAMA, FSA data area.
- AR6 - The increment code is initialized to 1. The address portion is initialized to the starting address of the CDDP data area.

INCREMENT REGISTERS

- INCR0 - 1024 Wrap. The increment value is set to -5.
- INCR1 - 1024 Wrap. The increment value is set to -2.
- INCR2 - 1024 Wrap. The increment value is set to +2.
- INCR3 - 1024 Wrap.
- INCR4 - 1024 Wrap. The increment value is set to +2.
- INCR5 - 1024 Wrap.
- INCR6 - 1024 Wrap.

BRANCH REGISTERS

- BNZA - Branch and Count Register controlling the number of executions of the main loop. Count and Reset fields are initialized to N-1, where N is the number of lines to be processed. The Branch Address is DSCLP.

SINE/COSINE DESTINATION REGISTERS

- SCD0 - Destine Cosine only to AE0.
- SCD1 - Destine Cosine/Sine to AE0.
- SCD2 - No-op (00).
- SCD3 - Destine Cosine/Sine to AE0.

DECIMATE REGISTER

Not Applicable.

SCALE FACTOR REGISTERS

- SFOH - All True-Direct.
- SFOL - Left and center prescalers - True/Right 1, right prescaler and postscaler - True/Direct.

NSWC TR 81-313

- SF1H - Left prescaler - True/Right 4, center and right prescalers - True/Right 2, postscaler True/Left 2.
- SF1L - All prescalers - True/Direct, postscaler - True/Left 4.
- SF2H - Left prescaler - True/Right 1, center and right prescalers - True/Direct, postscaler - True/Left 1.
- SF2L - All prescalers - True/Direct, postscaler - True/Left 2.
- SF3H - Left prescaler - True/Right 2, center prescaler - True/Direct, right prescaler - True/Right 1, postscaler - True/Left 1.
- SF3L - Left and center prescalers - True/Right 2, right prescaler - True/Direct, postscaler - True/Left 2.

ARITHMETIC ELEMENT REGISTER MAP

See Table 3-3.

WORKING STORE MAP

See Table 2-4. (BBAMP and DSCLN are combined.)

PROGRAM CODING CHART

See Table 3-4.

TABLE 3-1 DSCLN AP MICROPROGRAM SCALING

LABEL	ADDER IN	MULTIPLIER IN	OUTPUT
INPUTS:			
CO/DP	H0, H14		
CDO	F0		
SL	H16 (L.O.HW)		
P	H16 (L.O.HW)		
A		H12	
FM		H12	
AM		H15	
FS		H8	
7		H17	
5		H18	
BM2R, BM2I	H12		
BM1R, BM1I	H12		
BOR, BOI	H12		
BP1R, BP1I	H12		
BP2R, BP2I	H12		
BP3R, BP3I	H12		
INTERMEDIATE RESULTS:			
S, C		H14	
Z, K		H14	
7, 5		H18	
A		H12	
7C		H16	
5S		H16	
CS		H14	

TABLE 3-1 (CONTINUED)

LABEL	ADDER IN	MULTIPLIER IN	OUTPUT
CS		H14	
AK	F10	H12	
AZ	F10	H12	
5SC		H15	
AKS	F10		
AZS	F10		
AKC	F10		
AZC	F10		
7CAK		H14	
7CAZ		H14	
5SCAK	F11		
5SCAZ	F11		
7CCSAK	F12		
7CCSAZ	F12		
7SSCAK	F12		
7SSCAZ	F12		
T1, T2	F11		
T3, T4	F11		
FSM	F4		
D4	F0		
SL	F0		
PP	F0		
NCD4/NCD	F0		
CDP4	F0		
NC	F-15		
CC	F-1		

TABLE 3-1 (CONTINUED)

[illegible]

TABLE 3-2 DSCLN AEC REGISTER MAP

Incr Code		Address Register				WS Wrap		Increment Register				Memory Address Register			
0	3	4				15		0	3	4	15				
0			27C8=Cos ⁻¹ (7)					0			FFB=-5	DSCLN			
1			2809=Sin ⁻¹ (5)					0			FFE=-2				
2								0			002				
3								0							
4	1		620=A(SL,P,CD0)					0			002				
5	1		6E8=A(FAMA,FSA)					0			0				
6	1		5BC=A(C00P)					0			0				
7															

Sin/Cos Destination Register

AE0 AE1 AE2 AE3

0	1	0	0		
1	1	1	0		
2	0	0	0		
3	1	1	0		

Decimate Register

Count Reset

--	--

Comments

N = # of lines.

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers

Branch Address		Count		Reset	Spare	Branch Address
0	15	0	78	15	16	21 22 31
0		8				
1		9				
2		A	N-1	N-1		DSCLP
3		B				
4		C				
5		D				
6		E				
7		F				

TABLE 3-3 DSCLN AE REGISTER MAP

MLR				MRR			
0H	FS	A	0L	0H	C,FM	S,FM	0L
1H	P1	5SC,NCD	1L	1H	K,AM	Z,AM	1L
2H	7CAK,7C	7CAZ,5S	2L	2H	AK,7	AZ,5	2L
3H	7,C,P	5,S,SL	3L	3H	CS	SS,P1	3L

ALIR				ACIR			
0H	BM2, BP2, NC		0L	0H	7CCSAK, CD0, TEMP		0L
1H	BM1 BP3		1L	1H	7CCSAZ, CD0P, TEMP		1L
2H	B0 FSM		2L	2H	5SCAK, 7SSCAK, TEMP		2L
3H	BP1 PP		3L	3H	5SCAZ, 7SSCAZ, P		3L

ARIR				AEOR			
0	ASK			0H	M2R,P2R M2I,P2I		0L
1	ASZ			1H	M1R,P3R,CD0 M1I,P3I,CD0		1L
2	ACK			2H	0R,C 0I,D4		2L
3	ACZ			3H	P1R,SL P1I,P		3L

SCALE FACTOR REGISTERS

AE0				AE1			
0H	0 0 0 0	1 1 0 0	0L	0H			0L
1H	3 2 2 2	0 0 0 3	1L	1H			1L
2H	1 0 0 1	0 0 0 2	2L	2H			2L
3H	2 0 1 1	2 2 0 2	3L	3H			3L

ALOR				ACOR				AROR			
0	CD0P			0	AK,CD			0	T1,D4,M1		
1	P1			1	AZ			1	T2		
2	7			2	5			2	T3,CD4		
3	CD0			3	P1,LM			3	T4,CC		

TABLE 3-4 DSCN PROGRAM CODING CHART

[illegible]

TABLE 3-4 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	M/R	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR
	DSCLP		AR6 +0							CD0 = CD0 + SL			2 NDC4	
			READ CD	1L NCD			3 PP			CDP4 = H(CDOP) + D4				
			AR4 +0			NC = P1 * NCD				OD = NCD4 * LM		0 CDP4		1 CD0
			WRITE CD0							CC = PP - CDP4 - D4				
			AR4 -1				0 NC			C = CD0 + FSM		1 CC		2 OD
		CS(1)	READ SL, P							$P = \frac{L(NC)}{2} + CC \frac{NCD}{4}$				
			AR6 +0							SL = LO(SL)				2H C
			WRITE CD							7				3 P
			AR4 +0			A = A * AM				5				3H SL
		CS(3)	WRITE SL, P	3H 7	0H C									
			AR0 -2	3L 5		7C = 7 * C								
			READ BM2		0L S	C = P1 * C		A						
			AR0 +1			S = P1 * S		7C						
			READ BM1	0L A	1H K	5S = 5 * S	0 BM2			7C				
			AR0 +1			AK = A * K				C = LO(C)				
			READ B0	2H 7C	1L Z		1 BM1			S = LO(S)				
			AR0 +1	3H C		AZ = A * Z				5S				
			READ BP1	3L S			2 B0			AK				
			AR5 +2	2L 5S		CS = C * S						0 AK		
			READ FAMA		2H AK	5SC = 5S * C	3 BP1			AZ				
			AR5 +1			7CAK = 7C * AK						1 AZ		
			READ FSA		2L AZ	SS = S * S				CS				

TABLE 3-4 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR
			AR2 +0			7CAZ=7C*AZ		7CAK 0		55C	OH			
			READ FM	0 FS-A	3H CS	AKS=AK*S		1 SS		7CAK	2L R			
			AR3 +0	1L SSC		AZS=AZ*S		0 7CAZ		SS	2L R			
			READ AM	2H 7CAK	0 FM	AKC=AK*C			0 ASK	7CAZ	2L R			
			AR4 +2		3L SS	7CCSAK=7CAK*CS			1 ASZ	T1=(ASK-AK)/2	2H R			
			READ SL,P	2L 7CAZ	1 FM	AZC=AZ*C			2 ACK	T2=(ASZ-AZ)/2	2H R		0 T1	
			AR4 +1			7CCSAZ=7CAZ*CS		0 7CCSAK		T3=(AK-AK)/2	2H R		1 T2	
			READ CDO	3 SL,P					3 ACZ	M2R=BM2R-7CCSAK	OH		2 T3	
			AR6 +1			55CAK=55C*AK		1 7CCSAZ		T4=(AZ-ACZ)/2	2H R			
			READ CD					0 CDO		M21=BM21-7CCSAZ	OH		3 T4	0H M2R
			ARU +1			55CAZ=55C*AZ		2 55CAK		CDO	OH			
			READ BP2					1 CD		M1R=BM1R-55CAK+T1	2H R			0L M2L
			AR0 +1					3 55CAZ		CD	OH			
			READ BP3				0 BP2			M11=BM11-55CAZ+T2	OH			1H M1R
			AR0 -5							OR=BOR+AK/2+ACK/2	2H R			
			WRITE M2				1 BP3			O1=BO1+AZ/2+ACZ/2	2H R			1L M1L
			AR0 +1							P1R=BP1R-AK/2-ASK/2	2H R			2H OR
			WRITE M1							P11=BP11-AZ/2-ASZ/2	2H R			2L O1
			AR0 +1			7SSCAK=7CAK*SS				P2R=BP2R+55CAK+T3	2H R			3H P1R
			WRITE O			7SSCAZ=7CAZ*SS				P21=BP21+55CAZ+T4	2H R			3L P1L
			AR0 +1			ESM=ES*FM		2 7SSCAK		P1	OH			0H P2R
			WRITE P1					3 7SSCAZ		P3R=BP3R+7SSCAK	OH			0L P2L

TABLE 3-4 (CONTINUED)

[illegible]

CHAPTER 4

SINGLE REAL FFT (SRFFT) MACRO

FUNCTIONAL DESCRIPTION

The SRFFT MACRO performs the complex multiplications required to allow the FFT to effect the transformation from real time series to single-sided spectra. SRFFT is implemented as a separate pass which must be executed on a single-sided spectrum before bit reversal, or as a last step after a forward transform and bit reversal to produce a single-sided spectrum. For $N = 1024$, 2048 time samples are produced from 1024 spectral samples or vice-versa, and the six passes (1 SRFFT, 5 FFT4) require 2.46 ms.

The computation involves pairs of complex samples from symmetrical locations in the data array, i. e., outputs $F_n + F_{N-n}$ are derived from inputs G_n and G_{N-n} . The computation requires the exponential $e^{\frac{j2\pi n}{2N}}$, which is generated by the Sin/Cos Generator.

MATHEMATICAL DESCRIPTION

The input array is denoted by G_n , $n=0, \dots, N-1$. The output array is denoted by F_n , $n=0, \dots, N-1$. The computations are broken into the following steps, where GR_i , GI_i , FR_i , FI_i , etc., denote the real and imaginary parts of $G_i + F_i$, respectively, and C_i and S_i the real and imaginary parts of the complex exponential $\exp(j2\pi \frac{i}{2N})$:

$$CR_i = (GR_{N-i} - GR_i)/2$$

$$CI_i = (GI_{N-i} - GI_i)/2$$

$$SCR_i = S_i * CR_i$$

$$CCR_i = C_i * CR_i$$

$$CCI_i = C_i * CI_i$$

$$SCI_i = S_i * CI_i$$

$$AR_i = (GR_{N-i} + GR_i)/2$$

$$AI_i = (GI_{N-i} + GI_i)/2$$

$$\begin{aligned}
 FR_i &= (SCR_i + CCI_i + AR_i/4)*4 \\
 FI_i &= (SCI_i - CCR_i + AI_i/4)*4 \\
 FR_{N-i} &= (-SCR_i - CCI_i + AR_i/4)*4 \\
 FI_{N-i} &= (SCI_i - CCR_i - AI_i/4)*4
 \end{aligned}$$

IMPLEMENTATION

The SRFFT MACRO consists of a sixteen-instruction prologue and an eight-instruction main loop. During the prologue, two minus-one's are created and placed in MLR.2H and MRR.1H to allow data to be recycled through the multiplier with only a sign change. The (N-i) output address counter AR.5 is artificially incremented by one to allow the first output to be effected in the main loop with a decrement associated with it. Also unique to the prologue is the computation for F_0 , which for a forward transform is $FR_0 = GR_0/2 + GIO/2$, and for an inverse transform is $FR_0 = GR_0$, $FI_0 = GR_0$. These are selectable by SF2H and SF2L.

Scaling is applied in the computation of AR, AI, CR, and CI (SFOL) to effect the overall factor of 1/2 that is required from input to output. In addition, SF1H is used to compensate for the effective scaling index difference of two that is introduced when CR and CI are multiplied by C and S. If an additional net scaling is desired, it may be effected by reducing the number of postscaler shifts in SF1H.

The main loop count control is based on BNZ8, with an outside loop counter BNZ9 to permit operation on arrays larger than 512 points.

SCALING

See Table 4-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 4-2.

ADDRESS REGISTERS

- ARO - The initial value is set to zero, including increment code.
- AR2 - The increment code is set to 1. The address portion is initialized to the starting address of the Input Array.
- AR3 - The increment code is set to 1. The address portion is initialized to the last address of the Input Array.
- AR4 - The increment code is set to 1. The address portion is initialized to the starting address of the Output Array.

NSWC TR 81-313

AR5 - The increment code is set to 1. The address portion is initialized to the last address of the Output Array.

INCREMENT REGISTERS

INCO - Set to 1/2N as BAM angle increment.

INC2, 3, 4, 5 - Wrap code must be set to 1024.

BRANCH REGISTERS

BNZB - Branch and Count Register controlling the number of executions of the inner loop. Count and Reset fields are initialized to $N/4-2$ and $N/4-1$, respectively, where N is the array size. The Branch Address is SRFLP.

BNZC - Branch and Count Register controlling the number of executions of the outer loop. Count and Reset fields are initialized to 1. The Branch Address is SRFLP.

SINE/COSINE DESTINATION REGISTERS

SCDO - Destine Sine/Cosine to AEO and AE1.

DECIMATE REGISTERS

Not applicable.

SCALE FACTOR REGISTERS

SFOH - All True/Direct.

SFOL - Left, center and right prescalers - True/Right 1, postscaler - True/Direct.

SF1H - Left prescaler - True/Direct, center prescaler - True/Right 2, right prescaler - True/Direct, postscaler - True/Left 2.

SF2H - Forward Transform: Left and center prescalers - True/Right 1, right prescaler and postscaler - True/Direct.

Inverse Transform: Left and center prescalers - Inhibit, right prescaler and postscaler - True/Direct.

SF2L - Forward Transform: Left prescaler - True/Direct, center and right prescalers - Inhibit, postscaler - True/Direct.

Inverse Transform: Left prescaler - True/Direct, center and right prescalers - Inhibit, postscaler - True/Direct.

NSWC TR 81-313

ARITHMETIC ELEMENT REGISTER MAP

See Table 4-3.

WORKING STORE MAP

See Table 4-4.

PROGRAM CODING CHART

See Table 4-5.

TABLE 4-1 SRFFT AP MICROPROGRAM SCALING[illegible]

TABLE 4-2 SRFFT AEC REGISTER MAP

Incr Code		Address Register				WS Wrap		Increment Register				Memory Address Register																								
		0	3	4		15			0	3	4		15																							
0		0	000						$\frac{1}{2N}$				SRFFT																							
1																																				
2		1	A(INPUT) = I					0					Sin/Cos Destination Register AE0 AE1 AE2 AE3 <table> <tr> <td>0</td><td>1</td><td>1</td><td>1</td><td>1</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr> <tr> <td>2</td><td></td><td></td><td></td><td></td></tr> <tr> <td>3</td><td></td><td></td><td></td><td></td></tr> </table>				0	1	1	1	1	1	0	0	0	0	2					3				
0	1	1	1	1																																
1	0	0	0	0																																
2																																				
3																																				
3		1	A(EOI) = I+N-1					0																												
4		1	A(OUTPUT) = 0					0					Decimate Register Count Reset <table> <tr> <td></td><td></td></tr> </table>																							
5		1	A(E00) = 0+N-1					0																												
6													Comments N = Number of Complex Points EOI = End of Input E00 = End of Output																							
7																																				

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers

Branch Address		Count	Reset	Spare	Branch Address	
0	15	0	78	1516	2122	31
0		8				
1		9				
2		A				
3		B	$\frac{N}{2} - 2$	$\frac{N}{2} - 1$		SRFLP
4		C	1	1		SRFLP
5		D				
6		E				
7		F				

TABLE 4-3 SRFRT AE REGISTER MAP

MLR				MRR			
0H	GR	GI	0L	0H	C	S	0L
1H	CR	CI	1L	1H	M1		1L
2H	M1		2L	2H	GRN	GIN	2L
3H	DUMMY READ		3L	3H			3L

ALIR				ACIR			
0H	GR		GI	0L	GRN		GIN
1H	MGR			1L	MGRN		
2H	SCR/MGI		2L	2H	CCR/MGIN		2L
3H	SC I		3L	3H	CQ I		3L

ARIR				AEOR			
0				0H	FR		FI
1				1H	FRN		FIN
2				2H			
3				3H			

SCALE FACTOR REGISTERS								
AE0				AE1				
0H	0	0	0	0	1	1	1	0L
1H	0	2	0	2				1L
2H	1	1	0	0	0	4	4	2L
3H	4	4	0	0	0	4	4	3L

ALOR				ACOR				AROR			
0				0	AR			0	GI0		
1				1	AI			1			
2				2				2			
3				3				3			

TABLE 4-4 SRFET WORKING STORE MAP

LWS (AEO, AEI)		RWS (AEO, AEI)	
Input G_N Array (1024 FW)	Output F_N Array (1024 FW)	Input G_N Array (1024 FW)	Output F_N Array (1024 FW)
000		400	
100		500	
200		600	
300		700	

TABLE 4.5 SRFFT PROGRAM CODING CHART

[illegible]

TABLE 4-5 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR	
	SWFLP		AR2 READ G	1H CR 1L CI		MGRN=MI*GRN MGIN=MI*GIN MGI=MI*GI		1 MGR	2 CCR	FR=SCR+CCI+AR FI=SCI-CCR+AI FRN=-SCR-CCI+AR FIN=SCI-CCR-AI	1H K 1H K 1H K 1H K				
			AR3 READ GN			CCI=C*CI SCI=S*CI SCR=S*CR CCR=C*CR MGR=MI*GR NOP		2 MGIN 2 MGIN 2 MGI 3 GN 3 SCI 2 SCR		AR=-MGR-MGRN AI=MGI-MGIN CR=GRN-GR CI=GIN+GI	1H K 1H K 1H K 1H K				
	BNZB	CS	AR4 WRITE F		2 GN				3 CCI			0 AR AI			
	BNZC		AR5 WRITE FN												
						CCR=C*CR MGR=MI*GR NOP STOP				CI=GIN+GI					

CHAPTER 5

SCALE AND ADD TWO ARRAYS (SCLA2) MACRO

FUNCTIONAL DESCRIPTION

SCLA2 scales an array X by a constant A, scales an array Y by a constant B, and combines the two scaled arrays on an element-by-element basis to form an output array Z. X, Y, and Z must be of the same number of elements N. The scaling coefficients A and B are obtained via the Sin/Cos Generator in order to avoid the requirement for two words of Working Store (WS). These must therefore be loaded from the corresponding CFCB as the ARCCOS (A) and the ARCCOS (B), respectively.

MATHEMATICAL DESCRIPTION

$$Z_i = A * X_i + B * Y_i; \quad i = 1, 2, \dots, N$$

where A and B are two scalars, and X_i , Y_i and Z_i are the i th elements of arrays X, Y and Z, respectively.

IMPLEMENTATION

SCLA2 is implemented with a six-instruction main loop which processes one pair of X's and one pair of Y's to form one pair of Z's. A twelve-instruction preamble obtains the coefficients A and B via the Sin/Cos Generator and loads the pipe with the first pairs of X's and Y's. Each pass through the main loop then stores one pair of Z's in the output array. Since the maximum count is 255, or 256 passes through the loop, an outside loop is required to permit array sizes N greater than 512 elements. The inside loop is controlled by BNZ8 and the outside loop is controlled by BNZ9.

SCALING

See Table 5-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 5-2.

ADDRESS REGISTERS

- ARO - ARCCOS(A), i. e., ARO is set to an angle α such that $\cos(\alpha) = A$.
- AR1 - ARCCOS(B).
- AR2 - The increment code is initialized to one. The address is initialized to the first address of the X array.
- AR3 - The increment code is initialized to one. The address is initialized to the first address of the Y array.
- AR4 - The increment code is initialized to one. The address is initialized to the first address of the Z array.

INCREMENT REGISTERS

Not applicable. Wrap codes must be 1024 for INC 2, 3, 4.

BRANCH REGISTERS

- BNZ8 - Branch and Count register controlling the inner loop. Reset and Count fields are initialized to $N/M-1$, where N is the number of elements in each of the arrays, and M is the number of times the outside loop is executed. Branch Address is SC2LP.
- BNZ9 - Branch and Count register controlling the number of executions of the outer loop. Reset and Count fields are initialized to $M-1$. Branch Address is SC2LP.

SINE/COSINE DESTINATION REGISTERS

- SCD0 - Destine Cosine only to both AEO and AE1.
- SCD1 - Destine Cosine only to both AEO and AE1.

DECIMATE REGISTER

Not applicable.

SCALE FACTOR REGISTERS

- SFOH - Left, center and right prescalers - True/Direct. Postscaler - True/Left 2.

ARITHMETIC ELEMENT REGISTER MAP

See Table 5-3.

NSWC TR 81-313

WORKING STORE MAP

See Table 5-4.

PROGRAM CODING CHART

See Table 5-5.

TABLE 5-1 SCLA2 AP MICROPROGRAM SCALING

[illegible]

• E. ...

TABLE 5-2 SCLA2 AEC REGISTER MAP

Incr Code				Address Register				WS Wrap				Increment Register				Memory Address Register			
				0	3	4	15					0	3	4	15				
0				0	000			0				0				SCLA2			
1				0	000			0				0							
2				1	A(X)			0				Sin/Cos Destination Register							
3				1	A(Y)			0											
4				1	A(Z)			0				Decimate Register							
5																			
6												Count Reset							
7																			

AE0 AE1 AE2 AE3							
0	1	0	1	0			
1	1	0	1	0			
2							
3							

--	--	--	--

Comments

N = # of data points to be processed.

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers









Branch Address		Count	Reset	Spare	Branch Address	
0	15	0	78	15 16 21	22	31
0		8	$N/4-1$	$N/4-1$		SC2LP
1		9	1	1		SC2LP
2		A				
3		B				
4		C				
5		D				
6		E				
7		F				

TABLE 5-3 SCLA2 AE REGISTER MAP

MLR				MRR			
0H	XH	XL	0L	0H	A	B	0L
1H	YH	YL	1L	1H			1L
2H	DUMMY		2L	2H			2L
3H			3L	3H			3L

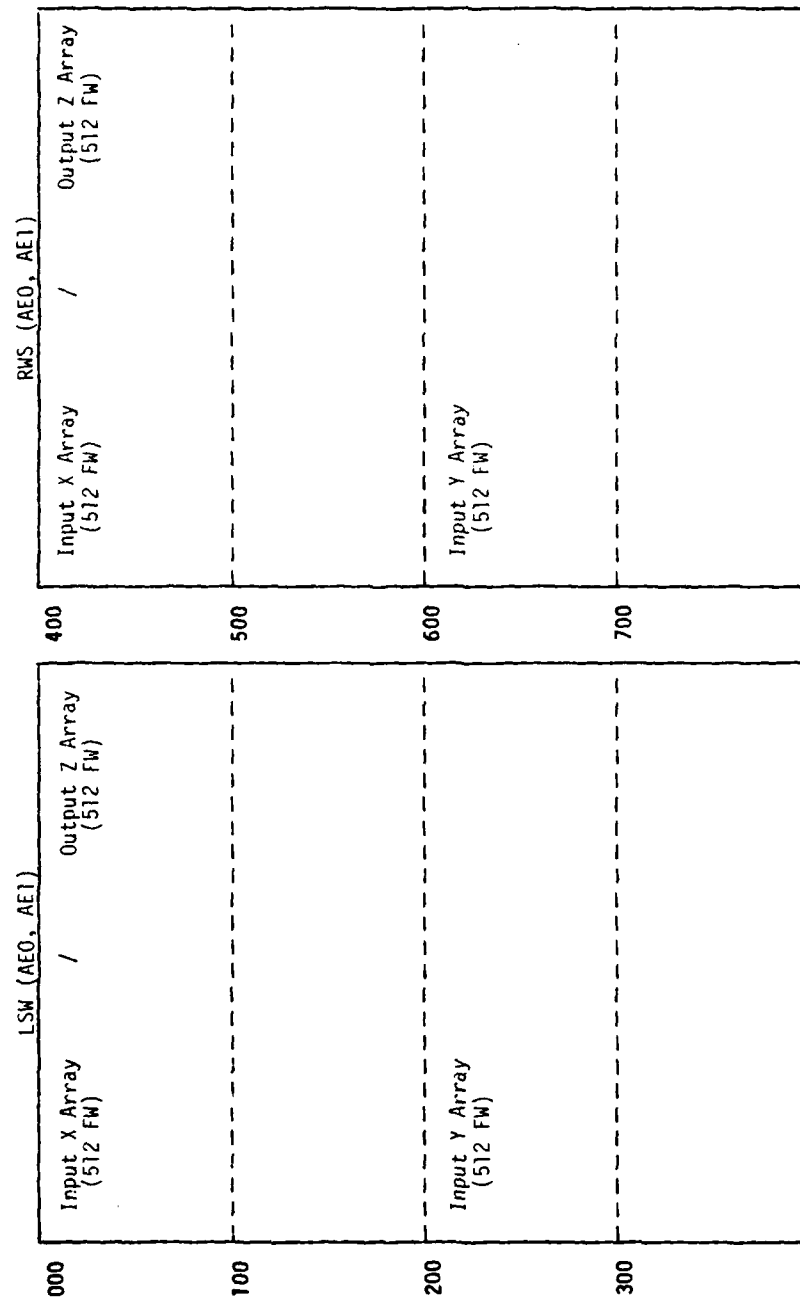
ALIR				ACIR			
0H	AX H		0L	0H	BX H		0L
1H	AX L		1L	1H	BX L		1L
2H			2L	2H			2L
3H			3L	3H			3L

ARIR				AEOR			
0				0H	ZH	ZL	0L
1				1H			1L
2				2H			2L
3				3H			3L

SCALE FACTOR REGISTERS											
AE0						AE1					
0H	0	0	0	2		0H	0	0	0	2	
1H						1H					
2H						2H					
3H						3H					

ALOR				ACOR				AROR			
0				0				0			
1				1				1			
2				2				2			
3				3				3			

TABLE 5-4 SCLA2 WORKING STORE MAP



[illegible]

TABLE 5-5 (CONTINUED)

[illegible]

CHAPTER 6

ASYNCHRONOUS SAMPLE, SCALE AND SUM (ASSSS) MACRO

FUNCTIONAL DESCRIPTION

The ASSSS MACRO performs the dopplered resampling of the input signal D for each multipath arrival at the sensor. Linear interpolation is employed to provide some protection against aliasing, and is equivalent to passing the signal through a filter with a frequency response of:

$$H(f) = \frac{\sin^2\left(\frac{\pi f}{f_s}\right)}{\left(\frac{\pi f}{f_s}\right)^2}$$

before resampling. The parameter f_s is the sample rate of the input or source signal. The resampled signal is multiplied by a gain parameter A and added to a Sum array S. Since there is not a one-to-one correspondence between the samples of the input signal D and the output, to add N new samples to the Sum array may require more or less than N samples of D. The resampling may start at an arbitrary phase (or fractional position F, $0 \leq F < 1$) with respect to the input samples, but the MACRO is intended for application only where the resample rate is relatively close to the original rate, say $\pm 10\%$ maximum.

MATHEMATICAL DESCRIPTION

Phase 1: Apply amplitude factor to source input samples

$$AH = A * DH$$

$$AL = A * DL$$

where A is the amplitude factor and DH and DL are the input samples in the high and low halves of the Working Store (WS) word.

Phase 2: Form interpolation fractions for next pair of outputs.

$$F1 = F2 + D + 0C$$

$$F3 = -F2 - D + 1C$$

$$F2 = F1 + D + 0C$$

$$F4 = -F1 - D + 1C$$

where D is the resample rate parameter, F1 and F2 are the resample fractions, F3 and F4 are the complements of F1 and F2, respectively, with respect to unity, and OC and LC are conditional "ones" that are used to constrain the F's to interval 0-1.

Phase 3: Form the products of the scaled inputs with the interpolation fractions.

$$1AH = F1 * AH$$

$$2AL = F2 * AL$$

$$3AL = F3 * AL$$

$$4AH = F4 * AH$$

Phase 4: Combine outputs of Phase 3 with sample values from Sum array to form final results.

For Inphase loop:

$$OH = SH + 3AL + 1AH$$

$$OL = SL + 4AH + 2AL$$

For Outphase loop:

$$OH = SH + 4AH + 2AL$$

$$OL = SL + 3AL + 1AH$$

IMPLEMENTATION

The ASSSS MACRO consists of two main loops, each eight instructions long, eight transition sequences for the eight possible ways that transitions between the two major loops can occur, plus some initialization and finalization code. If the block size is 1024 samples (512 words), both the input array and the output array may exceed 512 words, and the MACRO must operate from one half of Working Store to the other half. Smaller block sizes may be handled within one side of WS.

The two main loops are designated the "Inphase" loop and the "Outphase" loop, depending on how the input array and output array are related. Actually, a more reasonable nomenclature might be "leading" and "lagging" loops, since for the "inphase" or "leading" loop, the two samples in an output data word are derived from the two samples in the input data word plus one contribution from the previous input data word. For the "outphase" or "lagging" loop, the output data samples are derived from the two samples in the input data word plus one contribution from the following input data word.

Since the transitions will occur at rates less than one in twenty or more times through the main loops, the timing is nominally determined by the eight steps per word for each of the main loops. For nominally 512 executions of one or the other of the main loops (1024 samples), the approximate execution time for the ASSSS MACRO is .41 ms.

The operation of the two main loops is illustrated in Figures 6-1 and 6-2. Each figure follows the two samples in one input word through the pipeline to the three output samples that they affect. Since the outputs contain terms that involve triple products of an interpolation fraction, an amplitude and the input data sample, two full trips through the pipeline are required, beginning with a read of the input word in the first trip through the loop and ending with the write of the last affected output in the fourth following pass through the loop. On the first pass through the pipeline, the input data samples are multiplied by the amplitude factor. Approximately concurrent with these first products being passed through the adder, the four appropriate interpolation fractions are generated and passed to the multiplier. On the second pass through the pipeline, the scaled samples are multiplied by the interpolation fractions and these triple products are combined with the corresponding Sum array samples to form the final composite output.

At the time the interpolation fractions F_i are formed, a test is made to determine whether they have progressed out of the range $0 \leq F_i < 1$. Depending on which of the two fractions $F1$ or $F2$ have exceeded the valid range, and whether the increment D is positive or negative, the program deviates through one of eight transition routines to resume operation in the alternate (inphase or outphase) loop. These transition routines re-adjust the appropriate interpolation fractions to the valid range and compute the one or two output values that do not conform to the procedures in the main loops. The following gives a brief description of each of the transition sequences.

PI001 In to Out On $F1$, D positive

At the time the branch is taken, the following quantities have been erroneously computed:

$$F1 = -1 + e$$

$$F3 = 1 - e - 2D$$

$$F2 = e + D$$

$$F4 = 1 - e - D$$

where D is the amount the fraction F is incremented each sample, and e is a small number between 0 and D . The following two transition outputs are computed:

$$OH = SH = e * AL + (1-e) * AH$$

$$(AH \text{ from current input})$$

READ	MULTIPLIER IN	MULTIPLIER IN	ADDER IN	MULTIPLIER IN	ADDER IN	ADDER IN	ADDER	AEOR WRITE
SHSL (0)	AL (0) = A * DL (0)	AL (0) F2	F2 = F1 + D PASS AL (0) F3 = 1 - F2 - D	F2 AL (0) F3	1AH (0) = F1 * AH (0)	SHSL (0) / 3AL (-1) 1AH (0)		
DHDL (2)	AR (1) = A * DH (1)	F3 AR (1)	F3 = F2 + D PASS AR (1) F4 = 1 - F3 - D	F3 AR (1) F4	4AH (0) = F4 * AH (0) 2AL (0) = F2 * AL (0)	4AH (0) 2AL (0)	OH (0) = SH (0) + 3AL (1) + 1AH (0)	OH (0)
SHSL (1)	AL (1) = A * DH (1)	F4 AL (1)	F4 = F3 + D PASS AL (1) F5 = 1 - F4 - D	F4 AL (1) F5	3AL (0) = F3 * AL (0) 1AH (1) = F3 * AH (1)	SHSL (1) / 3AL (0) 1AH (1)	OL (0) = SH (0) + 4AH (0) + 2AL (0)	OL (0)
DHDL (3)	AR (2) = A * DH (2)	F5 AR (2)	F5 = F4 + D PASS AR (2) F6 = 1 - F5 - D	F5 AR (2) F6	4AH (1) = F4 * AH (1) 2AL (1) = F2 * AL (1)	4AH (1) 2AL (1)	OH (1) = SH (1) + 3AL (0) + 1AH (1)	OH (1)
SHSL (2)		F6 AR (2)	F6 = F5 + D PASS AR (2) F7 = 1 - F6 - D	F6 AR (2) F7	3AL (1) = F3 * AL (1) 1AH (2) = F1 * AH (2)	3AL (1) 1AH (2)	OH (2) = SH (2) + 3AL (1) + 1AH (2)	OH (2)

NOTE: SHADED AREA IS ONE CYCLE THROUGH THE INPHASE LOOP

FIGURE 6-1 ASSSS INPHASE MAIN LOOP FLOW

READ	MULTIPLIER IN	MULTIPLIER IN	ADD IN	MULTIPLIER IN	MULTIPLIER IN	ADD IN	ADD IN	ADD IN	AEOR WRITE
SHSL(1)	AL(0)	AL(0)	PASS AL(0) F3-1-F2-D	AL(0)	4AH(0)=F4*AH(0) 2AL(0)=F2*AL(0)	SHSL(0)/4AH(0) 2AL(0)			
SHSL(0)	AL(1)	AL(1)	PASS AL(1) F4-1-F3-D	AL(1)	3AL(0)=F3*AL(0) 1AH(1)=F1*AH(1)	3AL(0) 1AH(1)			
DHDL(2)	AL(2)	AL(2)	PASS AL(2) F3-1-F2-D	AL(2)	4AH(1)=F4*AH(1) 2AL(1)=F2*AL(1)	SHSL(1)/4AH(1) 2AL(1)			
SHSL(1)	AL(3)	AL(3)	PASS AL(3) F4-1-F3-D	AL(3)	3AL(1)=F3*AL(1) 1AH(2)=F1*AH(2)	3AL(1) 1AH(2)			
DHDL(3)	AL(4)	AL(4)	PASS AL(4) F3-1-F2-D	AL(4)	4AH(2)=F4*AH(2) 2AL(2)=F2*AL(2)	SHSL(2)/4AH(2) 2AL(2)			
SHSL(2)	AL(5)	AL(5)	PASS AL(5) F4-1-F3-D	AL(5)	3AL(2)=F3*AL(2) 1AH(3)=F1*AH(3)	3AL(2) 1AH(3)			

NOTE: SHADED AREA IS ONE CYCLE THROUGH THE OUTPHASE LOOP

FIGURE 6-2 ASSSS OUTPHASE MAIN LOOP FLOW

and $OL = SL + (e+D) * AH + (1-e-D) * AL$ (AH from next input)

which, using the fractional quantities already computed, become

$$OH = SH + F1 * AL - F1 * AH + AL$$

and $OL = SL - F2 * AH - F4 * AL$

Finally, the next interpolation fractions are computed

$$F2 = e + 2D$$

$$F4 = 1 - e - 2D$$

and computation resumes in the Outphase loop at MOPL2.

PI002 In to Out On F2

At the time the branch is taken, the following quantities have been erroneously computed:

$$F2 = -1 + e$$

$$F4 = -e$$

$$F1 = e + D$$

$$F3 = 1 - e - D$$

The transitional outputs become

$$OL = SL + e * AH + (1-e) * AL \quad (\text{previous AL})$$

$$\text{or } OL = SL - F4 * AH - F2 * AL$$

$$\text{and } OH = SH + (e+D) * AL + (1-e-D) * AH \quad (\text{current AL})$$

$$\text{or } OH = SH + F1 * AL + F3 * AH$$

The adjusted interpolation fractions are:

$$F2 = e + 2D$$

$$F4 = 1 - e - 2D$$

Computation resumes at MOPL1 in the Outphase loop.

POI01 Out to In On F1

At the time the branch is taken, the following quantities have been erroneously computed:

$$F1 = -1 + e$$

$$F3 = -e$$

$$F2 = e + D$$

$$F4 = 1 - e - D$$

The transition output is

$$OL = SL + e * AL + (1-e) * AH$$

$$\text{or } OL = SL - F3 * AL - F1 * AH$$

and the adjusted interpolation fractions are

$$F1 = e + D$$

$$F3 = 1 - e - D$$

Computation resumes at MIPL1 in the Inphase loop.

POI02 Out to In On F2

Erroneously computed fractions are:

$$F2 = -1 + e$$

$$F4 = 1 - e - 2D$$

$$F1 = e + D$$

$$F3 = 1 - e - D$$

The transition output is:

$$OH = SH - e * AH + (1-e) * AL \quad (AL \text{ from previous input})$$

$$\text{or } OH = SH + F2 * AH + AH - F2 * AL$$

The adjusted interpolation fractions are:

$$F1 = e + 2D \quad F3 = 1 - e - 2D$$

Computations resume at MIPL2 in the Inphase loop.

The four transition sequences for negative fraction increment D all produce transition outputs which are not exact. Each of the outputs is in error by a term involving a fraction factor that has a magnitude of (-2D) or less. Since by definition D is much less than unity, this term can safely be ignored. The alternative would have required long transition sequences involving "backing up" the computations to obtain data which is no longer in the pipeline.

MI001 In to Out On F1, D negative

At the time the branch is taken, the following quantities have been erroneously computed:

$$\begin{aligned} F1 &= -e & F2 &= 1 - e + D \\ F3 &= -1 + e & F4 &= e - D \end{aligned}$$

The transition outputs are:

$$\begin{aligned} OH &= SH - F3 * AL \\ &= SH + (1-e) * AL \\ (OH &= SH + (1-e) * AL + e * AH \text{ is exact}) \end{aligned}$$

and

$$\begin{aligned} OL &= SL + F2 * AH \\ &= SL + (1-e+D) * AH \\ (OL &= SL + (1-e+D) * AH + (e-D) * AL \text{ is exact}). \end{aligned}$$

The adjusted interpolation fractions are:

$$\begin{aligned} F4 &= e - 2D & F3 &= e - 3D \\ F2 &= 1 - e + 2D \end{aligned}$$

Computation resumes at MOPL1 in the Outphase loop.

MI002 In to Out On F2, D negative

At the time the branch is taken, the following quantities have been erroneously computed:

$$\begin{aligned} F2 &= -e & F4 &= -1 + e \\ F1 &= 1 - e + D & F3 &= e - D \end{aligned}$$

The transition output is:

$$\begin{aligned}
 OL &= SL - F4 * AH \\
 &= SL + (1-e) * AH \\
 (OL &= SL + (1-e) * AH + e * AL \text{ is exact}).
 \end{aligned}$$

The adjusted interpolation fractions are:

$$F2 = 1 - e + D \qquad F3 = e - 2D$$

Computation resumes at MOPL1 in the Outphase loop.

MOI01 Out to In On F1, D negative

At the time the branch is taken the following quantities have been erroneously computed:

$$\begin{aligned}
 F1 &= -e & F3 &= -1 + e \\
 F2 &= 1 - e + D & F4 &= e - D
 \end{aligned}$$

The transition output is:

$$\begin{aligned}
 OL &= SL - F3 * AL \\
 &= SL + (1-e) * AL \\
 (OL &= SL + (1-e) * AL + e * AH \text{ is exact}).
 \end{aligned}$$

The adjusted interpolation fractions are:

$$\begin{aligned}
 F4 &= e - 2D \\
 F1 &= 1 - e + D
 \end{aligned}$$

Computation resumes at MIPL1 in the Inphase loop.

MI002 Out to In On F2, D negative

At the time the branch is taken the following quantities have been erroneously computed:

$$\begin{aligned}
 F4 &= -1 + e & F2 &= -e \\
 F3 &= e - D & F1 &= 1 - e + D \\
 F4 &= e - 2D
 \end{aligned}$$

The transition outputs are:

$$\begin{aligned}
 OH &= SH - 4AH \\
 &= SH + (1-e) * AH \\
 (OH &= SH + (1-e) * AH + e * AL \text{ is exact}) \\
 \text{and } OL &= SL + 1AL \\
 &= SL + (1-e+D) * AL \\
 (OL &= SL + (1-e+D) * AL + (e-D) * AH \text{ is exact}).
 \end{aligned}$$

The adjusted interpolation fractions are:

$$\begin{aligned}
 F1 &= 1 - e + 2D \\
 F4 &= e - 3D
 \end{aligned}$$

Computation resumes at MIPL1 in the Inphase loop.

SCALING

See Table 6-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 6-2.

ADDRESS REGISTERS

- AR0 - The increment code is set to one. The address field is initialized to the location of the gain parameter A.
- AR1 - The increment code is set to one. The address field is initialized to the location of the F and D parameters.
- AR2 - The increment code is set to one. The address field is initialized to the location of the resampled input.
- AR3 - The increment code is set to one. The address field is initialized to the location of the sum input.
- AR4 - The increment code is set to one. The address field is initialized to the location of the resampled output.

INCREMENT REGISTERS

Not applicable. Wrap codes must be 1024 for INC 2, 3, 4.

BRANCH REGISTERS

- BCR0 - Conditional branch. For D positive, branch to PI001 on F1. For D negative, branch to MI001 on F1.
- BCR1 - Conditional branch. For D positive, branch to PI002 on F2. For D negative, branch to MI002 on F2.
- BR2 - Unconditional branch to MIPL2.
- BR3 - Unconditional branch to MOPL2.
- BCR4 - Conditional branch. For D positive, branch to POI01 on F1. For D negative, branch to MOI01 on F1.
- BCR5 - Conditional branch. For D positive, branch to POI02 on F2. For D negative, branch to MOI02 on F2.
- BR6 - Unconditional branch to MIPL1.
- BR7 - Unconditional branch to MOPL1.
- BNZ8 - Branch and Count register controlling the number of executions of

the Inphase processing loop. The Branch Address is MIPLP.
BNZ9 - Branch and Count register controlling the number of executions of
the Outphase processing loop. The Branch Address is MOPLP.
BNZA - Unconditional branch to MIPLO.
BNZB - Unconditional branch to MOPLO.
BNZC - Unconditional branch to STOP.

SINE/COSINE DESTINATION REGISTERS

Not applicable.

DECIMATE REGISTER

Not applicable.

SCALE FACTOR REGISTERS

SFOH - All True/Direct.
SFOL - All prescalers - True/Direct. Postscaler - True/Left 1.
SF1H - Left prescaler - True/Right 4; center and right prescalers -
True/Direct; postscaler - True/Left 4.

ARITHMETIC ELEMENT REGISTER MAP

See Table 6-3.

WORKING STORE MAP

See Table 6-4.

PROGRAM CODING CHART

See Table 6-5.

TABLE 6-1 ASSSS AP MICROPROGRAM SCALING

[illegible]

TABLE 6-2 ASSSS AEC REGISTER MAP

Incr Code		Address Register				WS Wrap		Increment Register				Memory Address Register			
0	3	4	15	0	3	4	15	0	3	4	15				
0	1	A(A)				0		0				MLP0 or MLPI			
1	1	A(F, D)				0		0							
2	1	A (Resample Input)				0		0				Sin/Cos Destination Register AE0 AE1 AE2 AE3			
3	1	A (Sum Input)				0		0							
4	1	A (Output)				0		0							
5															
6												Decimate Register Count Reset			
7															

BR/BCR Unconditional/ Conditional Branch		BNZ Branch and Count Registers			
Branch Address		Count	Reset	Spare	Branch Address
0	15	0	7	8	31
0	(I001)	8	CI	CI	MIPLP
1	(I002)	9	CO	CO	MOPLP
2	MIPL2	A	X'FF'	X'FF'	MIPL0
3	MOPL2	B	X'FF'	X'FF'	MOPL0
4	(OI01)	C	X'FF'	X'FF'	STOP
5	(OI02)	D			
6	MIPL1	E			
7	MOPL1	F			

Comments

For Out Phase start,
MAR = MLP0

For In Phase start,
MAR = MLPI

For D Positive,
BR0 = PI001
BR1 = PI002
BR4 = POI01
BR5 = POI02

For D Negative
BR0 = MI001
BR1 = MI002
BR4 = MOI01
BR5 = MOI02

TABLE 6-3 ASSSS AE REGISTER MAP

MLR

0H	DH	DL	0L
1H	F1	F3	1L
2H	F2	F4	2L
3H	DAL		3L

MRR

0H	AH	AL	0L
1H	A	-1	1L
2H			2L
3H			3L

ALIR

0H	DH	DL	0L
1H	SH	SL	1L
2H	F		2L
3H	D		3L

ACIR

0H	1AH		0L
1H	2AL		1L
2H	A	-1	2L
3H	1AH		3L

ARIR

0	3AL/1AL
1	4AH/2AH
2	AH
3	AL/FAL

AEOR

0H	OH	OL	0L
1H			1L
2H			2L
3H			3L

SCALE FACTOR REGISTERS

AE0

0H	0 0 0 0	0 0 0 3	0L
1H	3 0 0 3		1L
2H			2L
3H			3L

AE1

0H	0 0 0 0	0 0 0 3	0L
1H	3 0 0 3		1L
2H			2L
3H			3L

ALOR

0	OT
1	
2	
3	

ACOR

0	F1
1	F2
2	F3
3	F4

AROR

0	0
1	ONE
2	ONE
3	0

TABLE 6-4 ASSSS WORKING STORE MAP

LSW (AEO, AEI)		RWS (AEO, AEI)	
000	V1, V2 (18 FW)	400	V1, V2 (18 FW)
012	F, D (72 FW)	412	F, D (72 FW)
100	Sum Input / Resampled Output	500	Sum Input / Resampled Output
200	Resample Input	600	Resample Input
300		700	

[illegible]

TABLE 6-5 (CONTINUED)

[illegible]

TABLE 6-5 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR
	MIPLP		AR4 +1	2H F2		AH = A*DH		1AH	0	F3 = -F2-D+1C				
	BCRT 1002		WRITE OHOL		0L AL	4AH = F4*AH				OH = SH+1AH+3AL		F3		
	MIPL0		AR2 +1	1L F3		2AL = F2*AL			2	F1 = F2+D+0C				
			READ DHDL						4Ar	SETCS		F1	0	0H
	MIPL3		AR3 +1	1H F1		AL = A*DL		2AL		F4 = -F1-D+1C				
	BNZ8		READ SHSL	0H AH		3AL = F3*AL	0			OL = SL+2AL+4AH		F4		
	MIPL1			F4		1AH = F1*AH			3	F2 = F1+D+0C				
	BCR0 1001						SHSL		3AL	SETCS		F2	1	0L
			AR4 +1	2H F2		NOP								
	BNZC		WRITE OHOL			NOP								
	STOP					STOP								

TABLE 6-5 (CONTINUED)

[illegible]

TABLE 6-5 (CONTINUED)

[illegible]

TABLE 6-5 (CONTINUED)

[illegible]

TABLE 6-5 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR
	M1001			F3						OH = SL-3AH F4 = -F2-D+ONE F2 = F2+D F2 = F2+D	1H 0H 0H 0H			
	BR7 MOPL1			F4		1AH = F2*AH						F2		0H
	BNZ9 MOPLP		AR3 READ SHSL	F2		AH = A*DH 4AH = F4*AH		1AH		F3 = -F2-D+ONE OL = SL+1AH	1H	2 F3		
	M1002		AR2 READ CHDL	F1										
	SR7 MOPL1			DHDL						F2 = F1	0H			
	BNZ9 MOPLP		AR3 READ SHSL	F2		AH = A*DH 4AH = F3*AH				F3 = -F1-D+ONE OL = SL-4AH	0H 1H	F2 F3		

TABLE 6-5 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MUR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOB
	M0101			F2										
										DAL = -AL				
	BK6 MPLP1			3H						F1 = F2				
	BKZ8 MPLP		AR3 READ SHSL	1H		AL = -J * DAL 3AL = F4 * AL				F4 = F4-D OL = SL-3AL		F1 F4		
	M0102			2L					3 AL	OH = SH-4AH				
				F4						DAL = -AL				
	BK6 MPLP1			3H		1AL = F1 * AL				F1 = F1+D				OH
	BKZ8 MPLP		AR3 READ SHSL	1H		AL = DAL *-1 3AL = F4 * AL			Ø 1AL	F4 = F4-D OL = SL+1AH+1AL		F1 F4		

CHAPTER 7

SCALE AND ADD THREE ARRAYS (SCLA3) MACRO

FUNCTIONAL DESCRIPTION

SCLA3 MACRO scales an array X by a constant A, scales an array Y by a constant B, scales an array Z by a constant C, and combines the three scaled arrays on an element-by-element basis to form an output array W. X, Y, Z, and W must be of the same number of elements N.

SCLA3 is intended to provide arbitrary linear mixing of three inputs, and for convenience, the coefficients A, B, and C are accessed by the AE from Working Store. Separate address registers are used for the four arrays, and the output may overwrite any of the three inputs or the scaling parameters A, B, and C.

MATHEMATICAL DESCRIPTION

$$W_i = A * X_i + B * Y_i + C * Z_i; \quad i = 1, 2, \dots, N$$

where A, B, and C are scalars, and X_i , Y_i , Z_i and W_i are the i^{th} elements of arrays X, Y, Z and W, respectively.

IMPLEMENTATION

SCLA3 is implemented with an eight-instruction main loop which processes one pair of X's, one pair of Y's and one pair of Z's to form one pair of W's. A twelve-instruction preamble loads the three coefficients from Working Store using Address Register AR0, and loads the pipe with the first pairs of inputs from the three input arrays. In addition, the preamble decrements the output Address Register AR4 by one to allow the first output to be written into the initial value of AR4. Each pass through the main loop then stores one pair of W's in the output array. The main loop is controlled by BNZ9.

SCALING

See Table 7-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 7-2.

ADDRESS REGISTERS

- AR0 - The increment code is set to 1. The address field is initialized to the location of the parameters A, B, and C.
- AR1 - The increment code is set to 1. The address field is initialized to the first address of the X array.
- AR2 - The increment code is set to 1. The address field is initialized to the first address of the Y array.
- AR3 - The increment code is set to 1. The address field is initialized to the first address of the Z array.
- AR4 - The increment code is set to 1. The address field is initialized to the first address of the W array.

INCREMENT REGISTERS

Not applicable. Wrap codes must be 1024 for INC 0 to 4.

BRANCH REGISTERS

- BNZ9 - Branch and Count Register controlling the main loop. Reset and Count fields are initialized to $N/2-1$, where N is the number of elements in each of the arrays. Branch Address field is set to SC3LP.

SINE/COSINE DESTINATION REGISTERS

Not applicable.

DECIMATE REGISTER

Not applicable.

SCALE FACTOR REGISTERS

- SFOL - Left, center and right prescalers - True/Direct. Postscaler - True/Left 4.

ARITHMETIC ELEMENT REGISTER MAP

See Table 7-3.

NSWC TR 81-313

WORKING STORE MAP

See Table 7-4.

PROGRAM CODING CHART

See Table 7-5.

TABLE 7-1 SCLA3 AP MICROPROGRAM SCALING[illegible]

TABLE 7-2 SCLA3 AEC REGISTER MAP

Incr Code			Address Register			WS Wrap Increment Register			Memory Address Register																			
0	3	4	15			0	3	4	15																			
0	1	000	A,B,C									SCLA3																
1	1	100	A(X)																									
2	1	200	A(Y)									<div>Sin/Cos Destination Register</div> <div>AE0 AE1 AE2 AE3</div> <table><tr><td>0</td><td></td><td></td><td></td></tr><tr><td>1</td><td></td><td></td><td></td></tr><tr><td>2</td><td></td><td></td><td></td></tr><tr><td>3</td><td></td><td></td><td></td></tr></table>	0				1				2				3			
0																												
1																												
2																												
3																												
3	1	300	A(Z)																									
4	1	100	OUTPUT A(W)																									
5																												
6												<div>Decimate Register</div> <div>Count Reset</div> <table><tr><td></td><td></td></tr></table>																
7																												
<div>Comments</div> <div>N = # of samples</div>																												

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers

Branch Address		Count		Reset	Spare	Branch Address
0	15	0	78	15	16 21 22	31
0		8				
1		9	N/2-1	N/2-1		SC3LP
2		A				
3		B				
4		C				
5		D				
6		E				
7		F				

TABLE 7-3 SCLA3 AE REGISTER MAP

MLR				MRR			
0H	X1	X2	0L	0H	A	B	0L
1H	Y1	Y2	1L	1H	C		1L
2H	Z1	Z2	2L	2H			2L
3H			3L	3H			3L

ALIR				ACIR			
0H	AX 1		0L	0H	BY 1		0L
1H	AX 2		1L	1H	BY 2		1L
2H	DUMMY		2L	2H			2L
3H			3L	3H			3L

ARIR				AEOR			
0	CZ1		0H	W1		W2	0L
1	CZ2		1H				1L
2			2H				2L
3			3H				3L

SCALE FACTOR REGISTERS							
AE0				AE1			
0H	0	0	0	3			0L
1H							1L
2H							2L
3H							3L

ALOR				ACOR				AROR			
0				0				0			
1				1				1			
2				2				2			
3				3				3			

TABLE 7-4 SCLA3 WORKING STORE MAP

LSW (AE0, AE1)	RMS (AE0, AE1)
<div>400</div> <div>401</div> <div>A</div> <div>C</div> <div>B</div>	<div>A</div> <div>C</div> <div>B</div>
<div>500</div> <div>Input X Array (256 FW)</div> <div>/</div> <div>Output W Array (256 FW)</div>	<div>Input X Array (256 FW)</div> <div>/</div> <div>Output W Array (256 FW)</div>
<div>600</div> <div>Input Y Array (256 FW)</div>	<div>Input Y Array (256 FW)</div>
<div>700</div> <div>Input Z Array (256 FW)</div>	<div>Input Z Array (256 FW)</div>

TABLE 7-5 SCLA3 PROGRAM CODING CHART

#	LARCL BRANCH	SIN COS	READ WRITE	M/R	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOB
	SCLA3		AR0 +0			NOP								
			READ A.B											
			AR0 +1		A.B	NOP								
			READ C											
			AR1 +0		C	NOP								
			READ X1.X2											
			AR2 +0	X1.X2		NOP								
			READ Y1.Y2			AX1 = A*X1								
			AR3 +0	Y1.Y2		AX2 = A*X2								
			READ Z1.Z2			BY1 = B*Y1	AX1							
			AR4 -1	Z1.Z2		BY2 = B*Y2	AX2							
	SC3IP		READ DUMMY			CZ1 = C*Z1		BY1						
			AR1 +1			CZ2 = C*Z2	DUMMY	BY2						
			READ X3.X4						CZ1					
			AR2 +1	X3.X4					CZ2	W1=AX1+BY1+CZ1				
			READ Y3.Y4			AX3 = A*X3				W2=AX2+BY2+CZ2				
	BH79		AR3 +1	Y3.Y4		AX4 = A*X4				R				PH
			READ Z3.Z4			BY3 = B*Y3	AX3			R				PL
			AR4 +1	Z3.Z4		BY4 = B*Y4	AX4							
			WRITE W1.W2			NOP								
						STOP								

CHAPTER 8

FILTER TWO AND SUM THREE ARRAYS (F2S3) MACRO

FUNCTIONAL DESCRIPTION

F2S3 MACRO provides filtering of two input arrays X and Y to produce filter outputs F and G, respectively, and then combines F and G with a third array S to form a new output array S. The two filters for the X and Y inputs are two-pole recursive with separately specifiable gain and pole position parameters. The parameters and the initial states of the two filters are obtained from Working Store. The final states of the filters are returned to the same locations in Working Store. Separate Address Registers are provided for each of the input arrays and the output array. The output array may overwrite any of the input arrays or the parameters, but not the filter states. All arrays must be of the same number of elements N. The output S may be passed through a final filter consisting of a single zero at $Z = +1$ (i. e., a zero at zero frequency). This option is controlled by a Scale Factor Registers 1H and 1L, with a "0101, 0010" giving no zero and a "0111, 0111" enabling the filter.

MATHEMATICAL DESCRIPTION

The two filtering operations are:

$$F_i = U * X_i + A * F_{i-1} + B * F_{i-2}; \quad i = 1, \dots, N$$

and

$$G_i = V * Y_i + C * G_{i-1} + D * G_{i-2}; \quad i = 1, \dots, N$$

F_0 , G_0 , F_{-1} , and G_{-1} are initialized by the preamble.

The summing operation is:

$$S_i = S_i + F_i + G_i; \quad i = 1, \dots, N.$$

X_i , Y_i , and S_i are the i^{th} elements of the X, Y, and S arrays respectively, and F_i and G_i are partial results resident only in the AE registers. F_{N-1} , G_{N-1} , F_N and G_N are returned to Working Store, overwriting the initial states.

IMPLEMENTATION

F22S3 is implemented with a twelve-instruction main loop, a twenty-two instruction preamble and a six-instruction clean-up sequence. The preamble loads the parameters from Working Store via Address Register AR1, loads the initial filter states via Address Register AR5, and loads the pipe with the first pairs of X's, Y's and S's. Each pass through the main loop then produces a pair of filtered F's, a pair of filtered G's, and combines these with a pair of input S's to produce a pair of output S's. The clean-up sequence returns the final filter states to Working Store and stops. The main loop is controlled by BNZ8.

SCALING

See Table 8-1.

The filter coefficients A, B, C and D are treated as H14 numbers. The gain coefficients U and V are treated as H12 numbers. Assuming the inputs X and Y and the filter states F and G to be H0, the partial results AF, BF, CG and DG then are scaled F14, and the modified inputs UX and VY are scaled F12. SFOL is used in forming new filter states and shifts the AF, BF, CG and DG terms right by two on input. Outputs saved in ACOR and AROR do not pass through the postscaler, and, therefore, are F12. Outputs passed back to the multiplier are shifted left by four to regain a scaling of H0.

The summing operation uses SFOH which right shifts the S input four to agree with the F and G inputs, and shifts the output left four to achieve a final output scaling of H0. The filter states passed to the output to be saved for the next execution of F22S3 are also shifted left four by SFOH.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 8-2.

ADDRESS REGISTERS

- AR0 - The increment code is set to 1. The address field is initialized to the beginning of the input S array.
- AR1 - The increment code is set to 1. The address field is initialized to the beginning of the parameters block.
- AR2 - The increment code is set to 1. The address field is initialized to the beginning of the input X array.
- AR3 - The increment code is set to 1. The address field is initialized to the beginning of the input Y array.

AR4 - The increment code is set to 1. The address field is initialized to the beginning of the output S array.

AR5 - The increment code is set to 1. The address field is initialized to the beginning of the filter states block.

INCREMENT REGISTERS

INCO through 5 - The wrap field should be set to 1024.

BRANCH REGISTERS

BNZ8 - Branch and Count Register controlling the main loop. Count and Reset fields are initialized to $N/2-1$, where N is the number of elements in each of the arrays. The Branch Address field is set to F22LP.

SINE/COSINE DESTINATION REGISTERS

Not applicable.

DECIMATE REGISTER

Not applicable.

SCALE FACTOR REGISTERS

SFOH - Left prescaler - True/Right 4, Center and Right prescalers - True/Direct, Postscaler - True/Left 4.

SFOL - Left prescaler - True/Direct, Center and Right prescalers - True/Right 2, Postscaler - True/Left 4.

SF1H - Left and center prescalers - True/Direct, Right prescaler - True/Right 1 or Inhibit, Postscaler - True/Left 4.

SF1L - Left prescaler - True/Direct, Center prescaler - True/Right 1 or Inhibit, Right prescaler - True/Direct, Postscaler - True/Left 4.

ARITHMETIC ELEMENT REGISTER MAP

See Table 8-3.

WORKING STORE MAP

See Table 8-4.

PROGRAM CODING CHART

See Table 8-5.

TABLE 8-1 F22S3 AP MICROPROGRAM SCALING

LABEL	ADDER IN	MULTIPLIER IN	OUTPUT
INPUTS:			
FH, FL		H12	
GH, GL		H12	
U, V		H12	
A, C		H14	
B, D		H14	
XH, XL		H12	
YH, YL		H12	
SH, SL	H12		
SSH, SSL	H12		
INTERMEDIATE RESULTS:			
UXH, UXL	F8		
VYH, VYL	F8		
AFH, AFL	F10		
BFH, BFL	F10		
CGH, CGL	F10		
DGH, DGL	F10		
FH, FL	F8	H12	
GH, GL	F8	H12	
SSH, SSL	F8		
OUTPUTS:			
FHO, FLO			H12
GHO, GLO			H12
SHO, SLO			H12

TABLE 8-2 F22S3 AEC REGISTER MAP

Incr Code	Address Register	WS Wrap	Increment Register	Memory Address Register
0	3 4	15	0 3 4	15
0	1 S's (Input)			F22S3
1	1 Parameter $\begin{pmatrix} AC \\ BD \\ UV \end{pmatrix}$			
2	1 X's			Sin/Cos Destination Register
3	1 Y's			AE0 AE1 AE2 AE3
4	1 S's (Output)			0
5	1 States $\begin{pmatrix} PC \\ GO \\ SSN \end{pmatrix}$			1
6				2
7				3
				Decimate Register
				Count Reset
				Comments
				N = # of Data Samples

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers

Branch Address	Count	Reset	Spare	Branch Address
0	15	0	78	15 16 21 22
0		8	$N/2-1$	$N/2-1$
1		9		
2		A		
3		B		
4		C		
5		D		
6		E		
7		F		

TABLE 8-3 F22S3 AE REGISTER MAP

MLR			
0H	XH	XL	0L
1H	YH	YL	1L
2H	A	C	2L
3H	B	D	3L

MRR			
0H	U	V	0L
1H			1L
2H	FH	FL	2L
3H	GH	GL	3L

| | | | |

ALIR			
0H	SH	SL	0L
1H	SSH	SSL	1L
2H	U X		2L
3H	V Y		3L

ACIR			
0H	Dummy		0L
1H			1L
2H	A F		2L
3H	C G		3L

| | | | |

ARIR			
0			
1			
2	BF		
3	DG		

AEOR			
0H	SHO	SLO	0L
1H	FHO	FLO	1L
2H	GH0	GLO	2L
3H		SSL	3L

| | | | |
| SCALE FACTOR REGISTERS | | | | | | | | | | | |

AE0											
0H	3	0	0	3	0	2	2	3	0L		
1H	0	0	1	4	3	0	1	4	0	3	1L
2H											2L
3H											3L

AE1											
0H	3	0	0	3	0	2	2	3	0L		
1H	0	0	1	4	3	0	1	4	0	3	1L
2H											2L
3H											3L

| | | | | | | | | | | | |

ALOR			
0			
1			
2			
3			

ACOR			
0	SSH		
1	FH		
2	FL		
3			

AROR			
0	SSL		
1	GH		
2	GL		
3			

TABLE 8-4 F22S3 WORKING STORE MAP

LWS (AEO, AE1)		RWS (AEO, AE1)	
000	Parameters (6 FW)	400	Parameters (6 FW)
002	Filter States (6 FW)	402	Filter States (6 FW)
00A		40A	
100	Input S Array (256 FW) / Output S Array (256 FW)	500	Input S Array (256 FW) / Output S Array (256 FW)
200	Input X Array (256 FW)	600	Input X Array (256 FW)
300	Input Y Array (256 FW)	700	Input Y Array (256 FW)

TABLE 8-5 F22S3 PROGRAM CODING CHART

#	LABEL BRANCH	STN COS	READ WRITE	MLR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR
	F22S3		AR5 +0											
			READ FO											
			AR5 +1											
			READ GO		2 FH, FL									
			AR1 +0											
			READ A, C		3 GH, GL									
			AR1 +1											
			READ B, D	2 A, C										
			AR1 +1											
			READ U, V	3 B, D		AFL=A*FL								
			AR2			CGL=C*GL			2 AFL					
			READ XH, XL		0 U, V	BFL=B*FH			3 CGL					
			AR3			DGH=D*GH			2 BFL					
			READ YH, YL	0 XH, XL					3 DGH					
			AR5 +1			UXH=U*XH								
			READ SSO	1 YH, YL		VYH=V*YH								
			AR0				2 UXH							
			READ J, L, S				SSH, SSH			FH=UXH+AFL+BFL				
			AR4			BFL=B*FL	3 VYH			PASS SSL		1 FH		
			READ DUMMY		2H FH	DGL=D*GL	0 SH, SL						0 SSL	
			AR2 +1			UXL=U*XL				GH=VYH+CGL+DGH				
			READ XH, XL			VYL=V*YL			0 DUMMY	FHO=FH			1 GH	

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NAVAL SURFACE WEAPONS CENTER SILVER SPRING MD
ARITHMETIC PROCESSOR (AP) MICROPROGRAMS FOR DASS.(U)
AUG 81 R H DAVIS, D M BREATHOUSE

F/G 9/2

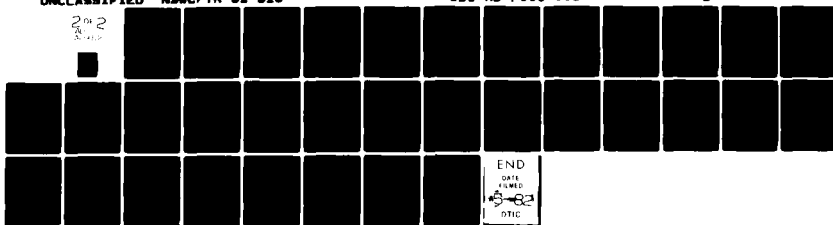
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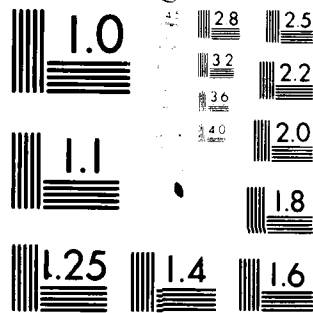
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MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

TABLE 8-5 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALTR	ACIR	ARIR	ADD	ALOR	ACOR	AROK	AEOR
	F22LP		AR3 +1		GH	AFH=A*FH	UXL 2			SSH=SH+FH+GH				
			READ YH,YL	XH,XL		CGH=C*GH	VYL 3			GH0=GH		SSH		1H FHO
						BFH=B*FH		AFH 2		SH0=SSH(-SSL)				
				1 YH,YL		DGH=D*GH		CGH 3		FL=UXL+AFH+BFL				2H GHO
						UXH=U*XH			BFH 2	GL=VYL+CGH+DGL		FL		0H SHO
					2L FL	VYH=V*YH			DGH 3	FLO=FL			GL 2	
			AR0 +1		GL	AFL=A*FL	UXH 2			SSL=SL+FL+GL				
			READ SH,SL			CGL=C*GL	VYH 3			GL0=GL			SSL 0	1L FLO
			AR2 +1			BFL=B*FL		AFL 2		SLO=SSL(-SSH)				
	BNZ8		READ XH,XL			DGL=D*GL	SH,SL 0	CGL 3		FH=UXH+AFL+BFL				2L GLO
			AR4 +1			UXL=U*XL			BFL 2	GH=VYH+CGL+DGH		FH 1		0L SLO
			WRITE SO	XH,XL	2H FH	VYL=V*YL			DGL 3	FHO=GH			GH 1	
										PASS SSL				
						NOP								
			AR5 +0											3L SSL
			WRITE SSO											
			AR5 -1			NOP								
			WRITE GO											
			AR5 -1			NOP								
			WRITE FO											
						NOP								
						STOP								

CHAPTER 9

DEMODULATED NOISE (DEMON) MACRO

FUNCTIONAL DESCRIPTION

The DEMON MACRO generates two channels of modulated broadband noise and adds the two on a sample-by-sample basis to a composite channel. Two channels of white noise are input to the MACRO which filters each with a two-pole recursive filter to provide some spectral shaping of the broadband noise. The modulating function for each channel is derived by truncating a sinusoid with arbitrary amplitude, mean and frequency.

MATHEMATICAL DESCRIPTION

DEMON computations are conveniently grouped into three phases:

- a) Generate Modulating Functions
- b) Generate Filtered Noises
- c) Form Composite Output Signal

Phase 1

For the first DEMON channel (AE0):

$$S_{1i} = \cos(ARO) \qquad ARO = ARO + INCO$$

For the first channel (AE1):

$$S_{1i} = \cos(AR2) \qquad AR2 = AR2 + INC2$$

where i is the time index.

The sinusoid is scaled by K

$$KS_{1i} = K_1 * S_{1i}$$

and then offset by $L_1 - T_1$ (Level - Threshold) to form a test parameter P_{1i} .

The modulating function value for the i^{th} sample is then given by

$$DM_{1i} = \begin{cases} T_1; & P_{1i} \leq 0 \\ KS_{1i} + L_i & P_{1i} > 0 \end{cases}$$

Similarly, for the second DEMON channel (AE0) and the second channel (AE1)

$$S_{2i} = \cos(AR1)$$

$$AR1 = AR1 + INC1$$

$$S_{2i} = \cos(AR3)$$

$$AR3 = AR3 + INC3$$

$$KS_{2i} = K_2 * S_{2i}$$

$$DM_{2i} = \begin{cases} T_2; & P_{2i} \leq 0 \\ KS_{2i} + L_2; & P_{2i} > 0 \end{cases}$$

Phase 2

For the first channel, the input white noise samples are passed through a two-pole recursive filter

$$Y_{1i} = A_1 * X_{1i} + B * Y_{1(i-1)} + C * Y_{1(i-2)}$$

where A_1 is a gain coefficient, B is equal to the TWOR filter coefficient and C is equal to the MRSQ coefficient. Similarly, for the second channel

$$Y_{2i} = A_2 * X_{2i} + B * Y_{2(i-1)} + C * Y_{2(i-2)}$$

Phase 3

The filtered noise channels are multiplied by the modulating functions

$$D_{1i} = DM_{1i} * Y_{1i}$$

$$D_{2i} = DM_{2i} * Y_{2i}$$

and combined with the composite channel to form the final output

$$TG_i = TG_i + D_{1i} + D_{2i}$$

IMPLEMENTATION

DEMON is implemented with a 20-instruction main loop, a 30-instruction preamble, and a 6-instruction clean-up. The preamble loads the registers and filter states from Working Store (WS) via Address Registers AR6 and AR7, generates the first two points of each periodic modulating signal via Address Registers AR0 through AR3, loads the first pair of channel inputs via Address Register AR4, and loads the first pair of target data via Address Register AR5. Since the target output overwrites the target input, a dummy read of -1 on AR5 is executed. Each pass through the main loop produces two pairs of filtered Y's which are multiplied by the corresponding modified modulating signals. The products are then added to the target signal to produce a composite output target signal. The cleanup sequence returns the final filter states to Working Store and stops. The main loop is

controlled by BNZF.

SCALING

See Table 9-1.

ARITHMETIC ELEMENT CONTROLLER (AEC) REGISTERS

See Table 9-2.

ADDRESS REGISTERS

- AR0 - Phase address for first DEMON channel (AE0).
- AR1 - Phase address for second DEMON channel (AE0).
- AR2 - Phase address for first DEMON channel (AE1).
- AR3 - Phase address for second DEMON channel (AE1).
- AR4 - The increment code is set to 1. The address field is initialized to the beginning of the input X array.
- AR5 - The increment code is set to 1. The address field is initialized to the beginning of the input TG array.
- AR6 - The increment code is set to 1. The address field is initialized to the beginning of the parameters array.
- AR7 - The increment code is set to 1. The address field is initialized to the beginning of the filter states array.
- INC0 - Frequency increment for the first DEMON channel (AE0).
- INC1 - Frequency increment for the second DEMON channel (AE0).
- INC2 - Frequency increment for the first DEMON channel (AE1).
- INC3 - Frequency increment for the second DEMON channel (AE1).
- INC4, 6, 7 - Wrap code must be set to 1024.
- INC5 - Wrap code - 1024, increment field - +2.

BRANCH REGISTERS

- BNZF - Branch and Count register controlling the number of executions of the main loop. Count and Reset fields are set to $N/2-1$, where N is the number of elements in the target array. The Branch Address is DMNLP.

SINE/COSINE DESTINATION REGISTERS

- SCD01 - Destine Cosine only to AE0.
- SCD23 - Destine Cosine only to AE1.

DECIMATE REGISTER

Not applicable.

SCALE FACTOR REGISTERS

SFOH - Left prescaler - True/Right 4, center and right prescalers - True/Direct, postscaler - True/Left 4.

SFOL - Left and center prescalers - True/Right 2, right prescaler - True/Direct, postscaler - True/Left 4.

SF1H - Left and center prescalers - True/Right 2, right prescaler - True/Direct, postscaler - True/Left 2.

SF1L - All - True/Direct.

ARITHMETIC ELEMENT REGISTER MAP

See Table 9-3.

WORKING STORE MAP

See Table 9-4.

PROGRAM CODING CHART

See Table 9-5.

TABLE 9-1 DEMON AP MICROPROGRAM SCALING

LABEL	ADDER IN	MULTIPLIER IN	OUTPUT
INPUTS:			
A1, A2		H12	
K1, K2		H12	
Y11, Y12		H12	
Y21, Y22		H12	
X11, X12		H13	
X21, X22		H13	
S		H14	
B, C		H14	
TG1, TG2	H7		
L1, T1	H12		
L2, T2	H12		
INTERMEDIATE RESULTS:			
AX1, AX2	F9		
BY'	F10		
CY1", CY2"	F10		
D1, D2	F8		
KS	F10		
Y		H12	
DM	H12		
P	F12		
OUTPUTS:			
Y11, Y12			H12
Y21, Y22			H12
TG1, TG2			H7

TABLE 9-2 DEMON AEC REGISTER MAP

Incr Code	Address Register	WS Wrap	Increment Register	Memory Address Register
0 3 4 15		0 3 4 15		
0	ANGLE 01		FREQ 01	DEMON
1	ANGLE 02		FREQ 02	
2	ANGLE 11		FREQ 11	Sin/Cos Destination Register
3	ANGLE 12		FREQ 12	
4	1 X1, X2	0		Decimate Register
5	1 T	0	+2	
6	1 Parameters	0		Count Reset
7	1 States	0		

Sin/Cos Destination Register

	AE0	AE1	AE2	AE3
0	1	0	0	0
1	1	0	0	0
2	0	0	1	0
3	0	0	1	0

Decimate Register

Count Reset

Comments

BR/BCR Unconditional/
Conditional Branch

BNZ Branch and Count Registers

Branch Address	Count	Reset	Spare	Branch Address
0 15	0 78	15 16	21 22	31
0	8			
1	9			
2	A			
3	B			
4	C			
5	D			
6	E			
7	F	FF	FF	DMNLP

TABLE 9-3 DEMON AE REGISTER MAP

MLR

0H	K1	A1	0L
1H	K2	A2	1L
2H	Y11	Y12	2L
3H	Y21	Y22	3L

MRR

0H	S	DM	0L
1H	B	C	1L
2H	X11	X12	2L
3H	X21	X22	3L

ALIR

0H	B Y'		0L
1H	TG1	TG2	1L
2H	L1	T1	2L
3H	L2	T2	3L

ACIR

0H	C Y1''		0L
1H	C Y2''		1L
2H	D 1		2L
3H	DUMMY		3L

ARIR

0	AX1
1	AX2
2	KS
3	D2

AEOR

0H	Y11	Y12	0L
1H	Y21	Y22	1L
2H	TG1	TG2	2L
3H			3L

SCALE FACTOR REGISTERS

AE0

0H	3	0	0	3	2	2	0	3	0L
1H	2	2	0	2	0	0	0	0	1L
2H									2L
3H									3L

AE1

0H	3	0	0	3	2	2	0	3	0L
1H	2	2	0	2	0	0	0	0	1L
2H									2L
3H									3L

ALOR

0	Y11
1	Y21
2	Y12
3	Y22

ACOR

0	T1
1	T2
2	
3	

AROR

0	P
1	0
2	
3	

TABLE 9-4 DEMON WORKING STORE MAP

LWS (AEO, AE1)		RWS (AEO, AE1)	
000	Input TG Array (256 FW)	400	Input TG Array (256 FW)
	Output TG Array (256 FW)		Output TG Array (256 FW)
100	Parameters (12 FW)	500	Parameters (12 FW)
180	Filter States (4 FW)	580	Filter States (4 FW)
200	Input X Array (512 FW)	600	Input X Array (512 FW)
300		700	

TABLE 9-5 DEMON PROGRAM CODING CHART

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALIR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOR
	DEMON		ARG +0			NOP								
			READ L1,T1											
			ARG +1			NOP								
			READ K1,A1				L1,T1							
			ARG +1							Pass T1				
			READ B1,C1	X1,A1										
			ARG +1											
			READ L2,T2		1									
			ARG +0		B1,C1									
			READ X11,X12				L2,T2							
	S(01)		ARG +0											
			READ Y11,Y12		2					Pass T2				
	S(11)		ARG +1		X11,X12									
			READ X2,A2											
			ARG +1											
			READ K2,X22											
	S(02)		ARG +1											
			READ Y21,Y22											
	S(12)		ARG +1											
			READ Y21,Y22											
			ARG +0											
	S(01)		READ T01,T02											

TABLE 9-5 (CONTINUED)

#	LABEL BRANCH	SIN COS	READ WRITE	MLR	MRR	MULTIPLY	ALTR	ACIR	ARIR	ADD	ALOR	ACOR	AROR	AEOB
			AR5 1			KS21 = K2*S21				P11 = L1-T1+KS11 Y11 = BY12+CV11 +AX11	1H		SETCS P11	
		S(11)	READ DUMMY			BY22 = B*Y22	1	CV21	1		0L			
						AX21 = A2*X21			2	DM11 = T1+(P11)C	1L			
		S(02)		Y11 2H	S12 0H	CV12 = C*Y12	0	DUMMY	3		R Y11			
					DM11	CV22 = C*Y22			AX21	P21 = L2-T2+KS21 Y21 = BY22+CV21 +AX21	1H			
		S(12)			S12	D11 = DM11*Y11		CV12	0		0L		SETCS P21	
						KS12 = K1*S12		CV22	1	DM21=T2+(P21)C	1L			
				Y21 3H	S22 0H	BY11 = B*Y11		D11	2	PASS Y11	0H R			
	DMNLP		AR4 1		DM21	AX12 = A1*X12	0		KS12					
		S(01)	READ X11, X12		S22	D21 = DM21*Y21	0			P12= L1-T1+KS12	1H		SETCS P12	Y11 0H
						KS22 = K2*S22			AX12	PASS Y21	0H			
		S(11)			X11, X12 2	BY21 = B*Y21			D21	Y12 = BY11+CV12 +AX12	0L			
						AX22 = A2*X22			KS22	DM12 = T1+(P12)C	1L			Y21 1H
		S(02)		Y12 2L	S11 0H	CV11 = C*Y11	0			P22 = L2-T2+KS22	1H Y12			
					DM12	CV21 = C*Y21			AX22	TG1 = TG1+D11+D21	1L		SETCS P22	
		S(12)			S11	D12 = DM12*Y12		CV11	0	Y22 = BY21+CV22 +AX22	0L			
						KS11 = K1*S11		CV21	1	DM22 = T2+(P22)C	1L			2H TG1
				Y22 3L	S21 0H	BY12 = B*Y12		D12	2	PASS Y12	0H R			
			AR4 1		DM22	AX11 = A1*X11			KS11					
		S(01)	READ X21, X22		S21	D22 = DM22*Y22	0			P11 = L1-T1+KS11	1H			Y12 0L
						KS21 = K2*S21			AX11	PASS Y22	0H		SETCS P11	
		S(11)			X21, X22 3	BY22 = B*Y22			D22	BY12+CV11 +AX11	0L			

TABLE 9.5 (CONTINUED)

[illegible]

NSWC TR 81-313

APPENDIX A

AP MICROPROGRAM SOURCE LISTINGS

RRRRRRRR	RRRRRRRR	RRRRRRRR	RR	RR	RRRRRRRR
RRRRRRRR	RRRRRRRR	RRRRRRRR	RRRR	RRRR	RRRRRRRR
RR	RR	RR	RR	RR	RR
RR	RR	RR	RR	RR	RR
RRRRRRRR	RRRRRRRR	RRRRRRRR	RR	RR	RRRRRRRR
RRRRRRRR	RRRRRRRR	RRRRRRRR	RR	RR	RRRRRRRR
RR	RR	RR	RR	RR	RR
RR	RR	RR	RR	RR	RR
RRRRRRRR	RRRRRRRR	RRRRRRRR	RR	RR	RR
RRRRRRRR	RRRRRRRR	RRRRRRRR	RR	RR	RR

*COMDECK BBAMP

* BB GENERATION 12/05/75 KMD

*

* 18 STEP PREAMBLE

BBAMP	AECW	LOG=0	M1 = NOT 0	A
	AECW2	RDWA=MLR.2,ALIR.2,AR.1,	READ AV1, COUNT1	*8
		TOMLR.0H	M1	
	AECW	LOG=0	M1 = NOT 0	0
	AECW2	RDWA=ALIR.3,AR.1,AAR,	READ DV1	*1
		TOMRR.0H	M1	
	AECW	SF.0H	NOP	2
	AECW2	RDWA=MRR.0,AR.0,	READ A1,A2	*3
		MLR.0H,MRR.0H	P1 = M1*M1	
	AECW	ALIR.3,SF.0H	DAV = DV1	4
	AECW2	TOACIR.0,TOAROR.0	P1. DAV	5
	AECW	MLR.2H,MRR.0H,	VA1 = AV1*A1	*6
		ALIR.2H,AROR.0,SF.0H	CAV2 = AV1 * DAV	
	AECW2	RDWA=MLR.3,AR.3,SAH,	BACK UP AR3	*7
		ACIR.0L,SF.0H,	P1 = LOW PART	*
		TOACOR.0,TOMLR.0L	CAV2	
	AECW	ALIR.2LC,SF.0H,	CT = -COUNT	*8
		TOARIR.0,	VA1	*
		TOAROR.1,ROUND	P1, ROUND CAV2	
	AECW2	RDWA=MRR.1,AR.2,	READ R1	*9
		MLR.0L,MRR.0L,	VA2=CAV2.A2	*
		TOACOR.1,	CT	*
		ARIR.0,SF.0L	PASS VA1	
	AECW	TOMLP.1H	VA1	10
	AECW2	RDWA=MRR.2,AR.2,AAR,	READ R2	*11
		TOARIR.0,ROUND	VA2,ROUND VA1	
	AECW	MLR.1H,MRR.1H,	BHR1=VA1,RR1	*12
		ARIP.0,SF.0L	PASS VA2	
	AECW2	RDWA=MRR.0,AR.0,AAR,	READ A3,A4	*13
		MLP.1H,MRR.1L,	BHI1=VA1,RI1	*
		ACOR.0,AROR.0,SF.0H,	CAV3=CAV2+DAV	*
		TOMLR.1L	VA2	
	AECW	TOALIR.0,	BHR1	*14
		TOACOR.0,TOMLR.0H,ROUND	CAV3,ROUND VA2	
	AECW2	MLR.1L,MRR.2H,	BHR2=VA2,RR2	*15
		TOALIR.1,ROUND,	BHI1,ROUND CAV3	*
		ACOR.0,AROR.0,SF.0H	CAV4=CAV3+DAV	
	AECW	MLP.0H,MRR.0H,	VA3=CAV3.A3	*16
		TOACOR.0,TOMLR.0L	CAV4	
	AECW2	MLR.1L,MRR.2L,	BHI2=VA2,RI2	*17
		TOACIR.0,TOAEOR.1,ROUND	BHR2,B1=0,ROUND CAV4	

NSWC TR 81-313

```

*
* 10 INSTRUCTION MAIN LOOP WITH EMBEDDED
* 9 INSTRUCTION-VARIATOR FUNCTION CHANGE
*
RR1  AECW  MLR,0L,MRR,0L,      VA4=CAV4,A4      *18
      TOARF,0,                VA3
      ACOR,1,AROR,1,SF,0H,    CT=CT+P1
      TOAEOR,1L,ROUND        B11, ROUND RR1
      AECW2 RDWR=MRR,1,AR,2,AAR, READ R3      *19
      TOACIR,1,ROUND,        B12,ROUND B11
      ARIP,0,SF,0L,          PASS VA3
      TOACOR,1,SETCS         CT,SET STATUS6
      AECW  TOARIP,0,         VA4      *20
      ACIR,0,ALIR,0C,SF,0L,  BR2=MRR2-BMR1
      TOMLR,1H               VA3
      AECW2 RDWR=MRR,2,AR,2,AAR, READ R4      *21
      ARIP,0,SF,0L,          PASS VA4
      TOAEOR,2H,ROUND,      BR2,ROUND VA3
      BCR,0                  BRANCH ON ST6
      AECW  MLR,1H,MRR,1H,    BMR3=VA3,RR3    *22
      TOMLR,1L,ROUND,        VA4,ROUND BR2
      ALIR,1,ACIR,1C,SF,0L   B12=B11-B12
      AECW2 RDWR=MRR,0,AR,0,AAR, READ A5,A6    *23
      MLR,1H,MRR,1L,        B13=VA3,R13
      TOAEOR,2L,ROUND,      B12,ROUND VA4
      ACOR,0,AROR,0,SF,0H   CAV5=CAV4+DAV
*
* VARIATOR FUNCTION CHANGE
* EXECUTES ONLY WHEN CT = 0
*
AECW  SF,0H,ROUND
AECW2 RDWR=ALIR,2,AR,1,AAR
AECW  SF,0H
AECW2 RDWR=ALIR,3,AR,1,AAR
AECW  SF,0H
AECW2 ALIP,2LC,SF,0H
AECW  MLR,1H,MRR,1H,
      ALIP,3,SF,0H,
      TOACOR,1
AECW2 MLR,1H,MRR,1L,
      ALIR,2H,SF,0H,
      TOAROR,0
*
* CONTINUATION OF MAIN LOOP
*
RR2  AECW  TOALIR,0,ROUND,    BMR3, ROUND B12    *32
      TOACOR,0,TOMLR,0H     CAV5
AECW2 MLR,1L,MRR,2H,        BMR4=VA4,RR4    *33
      TOALIR,1,ROUND,      B13,ROUND CAV5
      ACOR,0,AROR,0,SF,0H,  CAV6=CAV5+DAV
      WRM=AEOR,1,AR,3,AAR,  WRITE B1
      BNZ,0                BR TO BR1
AECW  MLR,0H,MRR,0H,        VAS=CAV5,A5    *34
      TOACOR,0,TOMLR,0L,    CAV6
      ALIR,0,ACIR,0C,SF,0L  BR3=BMR3-BMR2
AECW2 MLR,1L,MRR,2L,        B14=VA4,R14    *35
      TOAEOR,1H,ROUND,      BR3,ROUND CAV6
      ALIR,1C,ACIR,1,SF,0L, B13=B12-B13
      TOACIR,0,            BMR4
      WRM=AEOR,2,AR,3,AAR  WRITE B2
*
* OUTSIDE LOOP FOR SIZE GREATER THAN 512
*
AECW  TOAEOR,1L,ROUND      B13,ROUND BR3    36
AECW2 BNZ,9,ROUND
AECW  MLR,0H,MRR,0H
AECW2 MLR,1L,MRR,2L,
      ALIR,1C,ACIR,1,SF,0L
*
AECW  SF,0H
AECW2 BR,4
AECW  SF,0H
AECW2 SF,0H
      NOP
      BRANCH TO SM11
      NOP
      NOP CONTINUE

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NSWC TR 81-313

000000000	000000000	000000000	00	00	00
0000000000	0000000000	0000000000	00	000	00
00	00	00	00	00	00
00	00	00	00	00	00
00	00	000000000	00	00	00
00	00	000000000	00	00	00
00	00	00	00	00	00
00	00	0	00	00	00
0000000000	0000000000	0000000000	0000000000	00	000
0000000000	000000000	000000000	0000000000	00	00

*COMDECK DSCLN

DSCLN	AECW	SF.0H	NOP	-2
	AECW2	LOG=0.	CREATE MINUS 1	*-1
		RDWR=AR.2,AR.5,	READ FAMA	*
		SCMR.2H=AR.1	GET (5(PARAMETER	
	AECW	LOG=0,TOMRR.0H,TOAROR.0	DES M1	0
	AECW2	RDWR=MLR.0,AR.5,PAR.	READ FS,A	*1
		TOMLR.1H	DES M1	
	AECW	SF.0H	NOP	2
	AECW2	RDWR=ACIR.1,AR.6,	READ C00P	*3
		SCMR.2H=AR.0.	GET (7(PARAMETER	*
		MLR.1H,MRR.0H	P1=M1*M1	
	AECW	SF.0H	NOP	4
	AECW2	RDWR=MLR.3,AR.4,TOALIR.0	READ SL,P,DES P1	5
	AECW	ACIR.1,SF.0H	PASS C00P	6
	AECW2	ALIR.0L,SF.0H,TOALOR.0.	P1=LO(P1), DES CD4	*7
		RDWR=MRR.0,AR.2	READ FM	
	AECW	ALIP.0L,SF.0H,TOMLR.1H,TOACOR.3	P1=LO(P1),DES P1	8
	AECW2	TOALOR.1,TOMRR.3L,	DES P1, P1	*9
		ACOR.3,ANOR.0,SF.3L.	LM=M1*P1(R2)	*
		RDWR=ACIR.0,AR.4,AAR	READ C00	
	AECW	MLR.1H,MRR.2H,	7=7*P1	*A
		TOACOR.3	DES LM	
	AECW2	MLR.1H,MRR.2L.	5=5*P1	*B
		ALOR.0,ACOR.3,LOG=N	D4=CNDP AND LM	
	AECW	TOACIR.2,TOAROR.0.	DES 7,DES D4	*C
		MLR.0H,MRR.0H,	FSM=FS*FM	*
		ACIR.0,SF.0H	PASS C00	
	AECW2	MLR.3H,MRR.3L,TOACIR.3,	SL=P1*SL, DES 5	*D
		ACIR.2L,SF.2H,TOALOR.3,	7=LO(7)*2,DES C00	*
		RDWR=MRR.1,AR.3	READ AM	
	AECW	TOALIR.2,	DES FSM	*E
		ACIP.3L,SF.0H,TOALOR.2	5=LO(5), DES 7	
	AECW2	TOACIR.2,TOACOR.2,	DES SL. 5	*F
		ALIP.2,SF.1H	FSM4=FSM(R4)	
	AECW	TOAROR.1	DES FSM4	G
	AECW2	MLR.2L,MRR.3L,	PP=P*P1	*H
		ACIR.0,AROR.1,SF.1H	NCD4=(C00+FSM4)(R2)	
DSCLP	AECW	TOAPOR.2,TOMLR.1L,	DES NCD4,NCD	*10
		ALOR.3,ACIR.2,SF.0H	C00=C00+SL	
	AECW2	TOAFOR.1,	DES C00	*11
		ACIP.1H,AROR.0,SF.3L,	CNP4=M(CNDP)+D4	*
		RDWR=AR.0,AR.6,TOALIR.3	READ CD, DES PP	
	AECW	ACUR.3,AROR.2,LOG=N,	0D=CD AND LM	*12
		TOACOR.0.	DES CNP4	*

NSWC TR 81-313

AECW2	MLR,1L,MRR,3L ALIR,3,ACOR,0C,AROR,0C,SF,0L, TOAFOR,2, WRM=AEOR,1,AR,4	NC=P1*NCD CC=PP-CDP4-D4 DES 0D WRITE CD0	*13 *
AECW	AROR,1,ACIR,0,SF,0H, TOALIR,0,TOACOR,1	C=CD0+FSM4 DES NC, CC	*14
AECW2	ALIR,0L,ACOR,1,AROR,2,SF,3H, RDWR=AR,2,AR,4,SAR, SCMR,0H=AK,1,TOAEOR,2H	P=L(NC)/2*CC+NCD4 READ SL, P COS,SIN (D), DES C	*15 *
AECW	ACIR,2L,SF,0H,TOAEOR,3	SL=LO(SL), DES P	16
AECW2	ALOR,2,SF,0H,TOAEOR,3H, WRM=AEOR,2,AR,6	PASS 7, DES SL WRITE CD	*17
AECW	MLR,0L,MRR,1H, ACOR,2,SF,0H,TOMLR,3H	A=A*AM PASS 5, DES 7	*18
AECW2	TOMLR,3L, WRM=AEOR,3,AR,4, SCMR,1H=AK,3	DES 5 WRITE SL, P COS,SIN (P)	*19 *
AECW	MLR,3H,MRR,0H,TOACIR,0	7*C, DES A	1A
AECW2	MLR,1H,MRR,0H, ACIR,0,SF,1L, RDWR=ALIR,0,AK,0,AIRO	P1*C=C PASS A READ BM2	*18 *
AECW	MLR,1H,MRR,0L,TOACIR,0, TOMLR,0L	S=P1*S, DES 7C DES A	*1C
AECW2	MLR,3L,MRR,0L,TOACIR,1, ACIR,0A,SF,0H,ROUND, RDWR=ALIR,1,AR,0,AAR	S*S, DES C PASS 7C, RND A READ HM1	*1D *
AECW	MLR,0L,MRR,1H,TOACIR,0, ACIR,1LA,SF,0H,TOMLR,2H	A*K, DES S C=LO(C), DES 7C	*1E
AECW2	ACIR,0LA,SF,0H,ROUND, TOMLR,3H,TOACIR,1, RDWR=ALIR,2,AR,0,AAR	S=LO(S), RND 7C DES C, SS READ B0	*1F *
AECW	MLR,0L,MRR,1L,TOACIR,0, ACIR,1A,SF,0H,TOMLR,7L	A*Z, DES AK PASS 5S, DES S	*20
AECW2	ACIR,0,SF,2L,TOMLR,2L, RDWR=ALIR,3,AR,0,AAR	PASS AK, DES 5S READ BP1	*21
AECW	MLR,3H,MRR,0L,TOACIR,0, TOACOR,0,TOMRR,2H,ROUND	C*S, DES AZ DES AK, RND 5S	*22
AECW2	MLR,2L,MRR,0H,ROUND, ACIR,0,SF,2L, RDWR=AR,2,AR,5,AIRE	5S*C, ROUND AK PASS AZ READ FMA, AMA	*23 *
AECW	MLR,2H,MRR,2H,TOACIR,0, TOACOR,1,TOMRR,2L	7C*AK, DES CS DES AZ	*24
AECW2	MLR,7L,MRR,0L,TOACIR,1, ACIR,0A,SF,2L,ROUND, RDWR=MLR,0,AR,5,AAR	S*S, DES 5SC PASS CS, RND AZ READ FS, A	*25 *
AECW	MLR,2H,MRR,2L,TOACIR,0, ACIR,1,SF,2H,TOMRR,3H	7C*AZ, DES 7CAK PASS 5SC, DES CS	*26
AECW2	MLR,3L,MRR,2H,TOACIR,1, ACIR,0,SF,2L,ROUND, TOMLR,1L, RDWR=MRR,0,AR,2	AK*S, DES 5S PASS 7CAK, RND CS DES 5SC READ FM	*27 *
AECW	MLR,3L,MRR,2L,TOACIR,0, ACIR,1A,SF,2L,TOMLR,2H,ROUND	AZ*S, DES 7CAZ PASS 5S,DES 7CAK,R 5SC	*28
AECW2	MLR,3H,MRR,2H,TOARIR,0, ACIR,0,SF,2L,TOMRR,3L,ROUND, RDWR=MRR,1,AR,3	AK*C, DES ASK PAS 7CAZ,DES 5S,R 7CAK*	*29
AECW	MLR,2H,MRR,3H,TOARIR,1, ACOR,0C,ARIR,0,SF,2H,	READ AM 7CAK*CS, DES AS7 T1=(ASK-AK)/2	*2A *

NSWC TR 81-313

AECW2	TOMLR,2L,ROUND	DES 7CAZ, RND 55	
	MLR,3H,MRR,2L,TOARIR,2,	AZ=C, DES ACK	*28
	ACOR,1C,ARIR,1,SF,2H,	T2=(ASZ-AZ)/2	*
	TOAROR,0,ROUND,	DES T1, RND 7CAZ	*
AECW	RDWR=MLR,3,AR,4,AIRE	WEAD SL, P	
	MLR,2L,MRR,3H,TOACIR,0,	7CAZ=CS,DES 7CCSAK	*2C
	ACOR,0,ARIR,2C,SF,2H,	T3=(AK-ACK)/2	*
	TOAROR,1	DES T2	
AECW2	ALIP,0H,ACIR,0C,SF,0H,	M2R=BM2R-7CCSAK	*2D
	TOARIR,3,TOAROR,2,	DES ACZ, T3	*
	RDWR=ACIR,0,AR,4,AAR	WEAD CD0	
AECW	MLR,1L,MRR,2H,TOACIR,1,	SSC=AK,DES 7CCSAZ	*2E
	ACOR,1,ARIR,3C,SF,2H,	T4=(AZ-ACZ)/2	*
	TOAEOR,0H	DES M2R	
AECW2	ALIR,0L,ACIR,1C,SF,0H,	M2I=BM2I-7CCSAZ	*2F
	TOAROR,3,ROUND,	DES T4,RND M2R	*
	RDWR=ACIR,1,AR,6,AAR	WEAD CD	
AECW	MLR,1L,MRR,2L,TOACIR,2,	SSC=AZ, DES 5SCAK	*30
	ACIR,0,SF,0H,TOAEOR,0L	PASS CD0, DES M2I	
AECW2	ALIR,1H,ACIR,2C,AROR,0,	MIR=BMIR-5SCAK+T1	*31
	SF,2H,TOALOR,3,ROUND,	DES CD0, RND M2I	*
	RDWR=ALIR,0,AR,0,AAR	READ BP2	
AECW	ACIR,1,SF,0H,TOACIR,3,TOAEOR,1H	PASS CD,DES 5SCAZ,MIR	32
AECW2	ALIP,1L,ACIR,3C,AROR,1,SF,2H,	M1I=BM1I-5SCAZ+T2	*33
	TOALOR,0,ROUND,	DES CD4,RND MIR	*
	RDWR=ALIR,1,AR,0,AAR	READ BP3	
AECW	ALIR,2H,ACOR,0,ARIR,2,SF,2H,	OR=HOR+AK/2+ACK/2	*34
	TOAEOR,1L	DES M1I	
AECW2	ALIR,2L,ACOR,1,ARIR,3,SF,2H,	O1=H0I+AZ/2+ACZ/2	*35
	TOAEOR,2H,ROUND,	DES OR, RND M1I	*
	WRM=AEOR,0,AR,0,AIRE	WHITE M2	
AECW	ALIP,3H,ACOR,0C,ARIR,0C,SF,2H,	P1R=BP1R-AK/2-ASK/2	*36
	TOAEOR,2L,ROUND	DES OI, RND OR	
AECW2	ALIP,3L,ACOR,1C,ARIR,1C,SF,2H,	P1I=BP1I-AZ/2-ASZ/2	*37
	TOAEOR,3H,ROUND,	DES P1R, RND OI	*
	WRM=AEOR,1,AR,0,AAR	WHITE M1	
AECW	MLR,2H,MRR,3L,	7CAK=SS	*38
	ALIP,0H,ACIR,2,AROR,2,SF,2H,	P2R=BP2R+SSCAK+T3	*
	TOAEOR,3L,ROUND	DES P1I, RND P1R	
AECW2	MLR,2L,MRR,3L,	7CAZ=SS	*39
	ALIP,0L,ACIR,3,AROR,3,SF,2H,	P2I=BP2I+SSCAZ+T4	*
	TOAEOR,0H,ROUND,	DES P2R, RND P1I	*
	WRM=AEOR,2,AR,0,AAR	WRITE 0	
AECW	ALOR,1,SF,0H,TOACIR,2,	PASS P1, DES 7SSCAK	*3A
	MLR,0H,MRR,0H,	FSM=FS*FM	*
	TOAEOR,0L,ROUND	DES P2I, RND P2R	
AECW2	ALIP,1H,ACIR,2,SF,0H,	P3R=BP3R+7SSCAK	*3B
	TOACIR,3,TOARR,3L,ROUND,	DES 7SSCAZ,P1,RND P2I	*
	WRM=AEOR,3,AR,0,AAR	WRITE P1	
AECW	ALIP,1L,ACIR,3,SF,0H,	P3I=BP3I+7SSCAZ	*3C
	TOALIR,2,TOAEOR,1H	DES FSM,P3R	
AECW2	MLR,3H,MRR,3L,	SL=P1*SL	*3D
	TOAEOR,1L,ROUND,	DES P3I, RND P3R	*
	WRM=AEOR,0,AR,0,AAR,	WHITE P2	*
	ALIR,2,SF,1H,	FSM4=FSM(R4)	*
	BNZ,A	RR ON CT TO USCLP	
AECW	ALOR,0,ACOR,3,LOG=N,	D4=CD0P AND LM	*3E
	TOAROR,1,ROUND	DES FSM4, RND P3I	
AECW2	TOACTR,2,TOAROR,0,	DES SL, D4	*3F
	ACIR,0,AROR,1,SF,1H,	NCD4=CD0+FSM4	*
	MLR,3L,MRR,3L,	PP=P1*P	*
	WRM=AEOR,1,AR,0,AAR	WHITE P3	
AECW	SF,0H	NOP	40
AECW2	STOP		41

NSWC TR 81-313

SSSSSSSS	SSSSSSSS	SSSSSSSSSS	SSSSSSSSSS	SSSSSSSSSS
SSSSSSSSSS	SSSSSSSSSS	SSSSSSSSSS	SSSSSSSSSS	SSSSSSSSSS
SS S	SS SS	SS	SS	SS
SS	SS SS	SS	SS	SS
SSSSSSSS	SSSSSSSSSS	SSSSSS	SSSSSS	SS
SSSSSSSS	SSSSSSSS	SSSSSS	SSSSSS	SS
SS	SS SS	SS	SS	SS
S SS	SS SS	SS	SS	SS
SSSSSSSSSS	SS SS	SS	SS	SS
SSSSSSSS	SS SS	SS	SS	SS

*COMDECK SRFFT

SRFFT	AECW	LOG=0	CREATE ALL ONES	0
	AECW2	TOMLR.2H.	M1=MINUS 1	*1
		RDWR=ALIR.1,AR.2	HEAD G0	
	AECW	LOG=0	NEED TWO M1S	2
	AECW2	TOMRR.1H.	M1	*3
		RDWA=MLR.0,ALIR.2,AR.2,AAH.	READ G1	*
		SCMP.0=AR.0,INC	GET COS,SIN (INC)	
	AECW	ALIR.1H,SF.0H	FR0=GR0	4
	AECW2	ALIR.1H,SF.0H.	F10=GR0	*5
		RDWR=ACIR.0,AR.3.	HEAD GN1	*
		TOAEO.0H	FR0	
	AECW	TOAFOR.0L	F10	6
	AECW2	RDWR=MLR.3,AR.5,AAH	DUMMY READ FOR FN	7
	AECW	ALIR.2L,ACIR.0L,SF.0L	CI1=(GIN1+GI1)/2	8
	AECW2	TOMLR.1L.	CI1	*9
		ALIR.2H,ACIR.0H,SF.0L.	AR1=(GRN1+GR1)/2	*
		RDWA=MLR.0,ALIR.0,AR.2,AAH	READ G2	
	AECW	TOACOR.0,ROUND.	AR1, ROUND CI1	*A
		ALIR.2HC,ACIR.0H,SF.0L	CR1=(GRN1-GR1)/2	
	AECW2	TOMLR.1H.	CH1	*B
		MLR.1L,MRR.0H.	CCI1=C*CI1	*
		ALIR.2LC,ACIR.0L,SF.0L.	AI1=(GIN1-GI1)/2	*
		RDWA=MRR.2,ACIR.0,AR.3,SAR	READ GN2	
	AECW	TOACOR.1,ROUND.	AI1, ROUND CH1	*C
		MLR.1L,MRR.0L	SCI1=S*CI1	
	AECW2	TOAIR.3.	CCR1	*D
		MLR.1H,MRR.0L.	SCR1=S*CR1	*
		WRM=AEOR.0,AR.4.	WRITE F0	*
		SCMP.0=AR.0,INC	COS,SIN (2*INC)	
	AECW	TOAIR.3.	SCI1	*E
		MLR.1H,MRR.0H.	CCR1=C*CR1	*
		ALIR.0HC,ACIR.0H,SF.0L	CR2=(GRN2-GR2)/2	
	AECW2	TOAIR.2,TOMLR.1H.	SCR1,CH2	*F
		ALIR.0L,ACIR.0L,SF.0L.	CI2=(GIN2+GI2)/2	*
		MLR.0H,MRR.1H	MGR2=M1*GR2	
SRFLP	AECW	TOAIR.2,TOMLR.1L,ROUND.	CCW,CI,ROUND CR	*10
		MLR.2H,MRR.2H.	MGRN=M1*GRN	*
		ALIR.2,ARIR.3,ACOR.0,SF.1H	FR=SCR*CCI+AR	
	AECW2	TOAIR.1,TOAEO.0H,ROUND.	MGR, FR, ROUND CI	*11
		MLR.2H,MRR.2L.	MGIN=M1*GIN	*
		ALIR.3,ARIR.2C,ACOR.1,SF.1H.	FI=SCI-CCR*AI	*
		RDWA=MLR.0,ALIR.0,AR.2,AAH	READ G	
	AECW	TOACIR.1,TOAEO.0L,ROUND.	MGRN, FI, ROUND FR	*12
		MLR.0L,MRR.1H.	MGI=M1*SI	*

NSWC TR 81-313

AECW2	ALIR.2C,AWIR.3C,ACOR.0,SF.1H	FRN=-SCR-CCI*AR	
	TOACIR.2,TOAEOR.1H,ROUND.	MGIN,FRN,ROUND FI	*13
	MLR.1L,MRR.0H,	CCI=C*CI	*
	ALIR.3,ARIP.2C,ACOR.1C,SF.1H,	FIN=SCI-CCR-AI	*
	RDWA=MRR.2,ACIR.0,AR.3,SAW	READ GN	
AECW	TOALIR.2,TOAEOR.1L,ROUND,	MGI,FIN,ROUND FRN	*14
	MLR.1L,MRR.0L,	SCI=S*CI	*
	ALIR.1LC,ACIR.1LC,SF.0L	AR=(-MGR-MGRN)/2	
AECW2	TOAPIR.3,TOACOR.0,ROUND,	CCI,AR,ROUND FIN	*15
	MLR.1H,MRR.0L,	SCR=S*CR	*
	ALIR.2L,ACIR.2LC,SF.0L,	AI=(MGI-MGIN)/2	*
	WRM=AEOR.0,AR.4,AAR,	WRITE F	*
	SCMR.0=AR.0INC.BNZ.B	COS,SIN,LOOP UN BNZB	
AECW	TOALIR.3,TOACOR.1,	SCI.AI	*16
	MLR.1H,MRR.0H,	CCR=C*CR	*
	ALIR.0HC,ACIR.0H,SF.0L	CR=(GRN-GR)/2	
AECW2	TOALIR.2,TOMLR.1H,	SCR,CR	*17
	MLR.0H,MRR.1H,	MGR=M1*GR	*
	ALIR.0L,ACIR.0L,SF.0L,	CI=(GIN+GI)/2	*
	WRM=AEOR.1,AR.5,SAW	WRITE FN	
AECW	SF.0H	NOP	18
AECW2	BNZ.C	OUTSIDE LOOP	19
AFCW	MLR.1H,MRR.0H	CCR=C*CR	14
AECW2	MLR.0H,MRR.1H,	MGR=M1*GR	*18
	ALIR.0L,ACIR.0L,SF.0L	CI=(GIN+GI)/2	
AECW	SF.0H	NOP	1C
AECW2	STOP	STOP	10

NSWC TR 81-313

SSSSSSSS	SSSSSSSS	SS	SSSSSSSS	SSSSSSSS
SSSSSSSSSS	SSSSSSSSSS	SS	SSSSSSSSSS	SSSSSSSSSS
SS S	SS S	SS	SS SS	S SS
SS	SS	SS	SS SS	SS
SSSSSSSS	SS	SS	SS SS	SS
SSSSSSSS	SS	SS	SSSSSSSS	SS
SS	SS	SS	SSSSSSSS	SS
S SS	SS S	SS	SS SS	SS
SSSSSSSS	SSSSSSSS	SSSSSSSS	SS SS	SSSSSSSS
SSSSSS	SSSSSS	SSSSSSSS	SS SS	SSSSSSSS

*COMDECK SCLA2

SCLA2	AECW	SF.0H	NOP	0
	AECW2	RDWR=MLR.0,AR.2,	READ 1ST PAIR OF XIS	*1
		SCMR.0H=AR.0	GENERATE PARAMETER A	
	AECW	SF.0H	NOP	2
	AECW2	RDWR=MLR.1,AR.3,	READ 1ST PAIR OF YIS	*3
		SCMR.0L=AR.1	GENERATE PARAMETER B	
	AECW	SF.0H	NOP	
	AECW2	SF.0H	NOP	
	AECW	MLR.0H,MRR.0H	AXH=A*XH	4
	AECW2	MLR.0L,MRR.0H,	AXL=A*XL	*5
		RDWR=MLR.2,AR.4,SAR	BACK UP Z POINTER	
	AECW	TOALIR.0,	AXH	*6
		MLR.1H,MRR.0L	HYH=B*YH	
	AECW2	TOALIR.1,	AXL	*7
		MLR.1L,MRR.0L,	BYL=B*YL	*
		RDWR=MLR.0,AR.2,AAR	READ NEXT PAIR OF XIS	
	AECW	TOACIR.0	BYH	8
	AECW2	RDWR=MLR.1,AR.3,AAR,	READ NEXT PAIR OF YIX	*9
		TOACIR.1	BYL	
	AECW	MLR.0H,MRR.0H,	AXH=A*XH	*A
		ALIR.0,ACIR.0,SF.0H	ZH=AXH+BYH	
	AECW2	MLR.0L,MRR.0H,	AXL=A*XL	*B
		ALIR.1,ACIR.1,SF.0H,	ZL=AXL+BYL	*
		TOAENR.0H	ZH	
SC2LP	AECW	MLR.1H,MRR.0L,	BYH=B*YH	*C
		TOAENR.0L,TOALIR.0	ZL, AXH	
	AECW2	RDWR=MLR.0,AR.2,AAR,	READ NEXT PAIR OF XIS	*D
		MLR.1L,MRR.0L,	BYL=B*YL	*
		TOALIR.1	AXL	
	AECW	TOACIR.0	BYH	E
	AECW2	RDWR=MLR.1,AR.3,AAR,	READ NEXT PAIR OF YIS	*F
		TOACIR.1,BNZ.8	RYL, BRANCH TO SC2LP	
	AECW	MLR.0H,MRR.0H,	AXH=A*XH	*10
		ALIR.0H,ACIR.0H,SF.0H	ZH=AXH+BYH	
	AECW2	WRM=AEOR.0,AR.4,AAR,	WRITE A PAIR OF ZIS	*11
		MLR.0L,MRR.0H,	AXL=A*XL	*
		ALIR.1,ACIR.1,SF.0H,	ZL=AXL+BYL	*
		TOAENR.0H	ZH	
	AECW	SF.0H	NOP	12
	AECW2	BNZ.9	OUTSIDE LOOP	13
	AECW	MLR.0H,MRR.0H	AXH=A*XH	14
	AECW2	MLR.0L,MRR.0H,	AXL=A*XL	*15
		ALIR.1,ACIR.1,SF.0H	ZL=AXL+BYL	
	AECW	SF.0H	NOP	16
	AECW2	STOP	STOP	17

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      AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA
      AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA
      AA      AA  AA      A  AA      A  AA      A  AA      A
      AA      AA  AA      AA  AA      AA  AA      AA  AA      AA
      AA      AA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA
      AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA
      AAAAAAAAAA  AA      AA  AA      AA  AA      AA  AA      AA
      AA      AA  A      AA  A      AA  A      AA  A      AA
      AA      AA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA
      AA      AA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA  AAAAAAAAAA

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*COMDECK ASSSS

* MLPTH - MULTIPATH RESAMPLE, SCALE AND ADD

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* MLPI

IN PHASE START SEQUENCE

RMD 01/26/76

AECW	SF.0H	NOP	0
AECW2	RDWA=MRR.1,ACIR.1,AR.0	READ A, -1	1
AECW	SF.0H	NOP	2
AECW2	RDWA=ALIR.2,AR.1	READ F	3
AECW	TOALOR.0,SF.0H	0 = INHIBIT	4
AECW2	RDWA=MLR.0,ALIR.0,AR.2,	READ DMHL (1)	*5
	TOAROR.0,SF.0H	0 TO 0C	
AECW	TOAROR.3,	0 TO 1C	*6
	ALOR.0C,AROR.0C,ACIR.1LC,SF.0H	ONE=-1 -EPS	
AECW2	RDWA=MLR.0,ALIR.0,AR.2,AAR,	READ DMHL (2)	*7
	TOAROR.1,	ONE TO 0C	*
	ALOR.0C,AROR.0C,ACIR.1LC,SF.0H	ONE=-1 -EPS	
AECW	MLR.0L,MRR.1H,	AL = A*DL	*8
	TOAROR.2	ONE TO 1C	
AECW2	RDWA=ALIR.3,AR.1,AAR	READ 0	9
AECW	MLR.0H,MRR.1H,	AM = A*DH	*10
	TOARIR.3,	AL	*
	ALIR.2C,AROR.1,SF.0H	F3 = ONE-F	
AECW2	ARIR.3,SF.0L,	PASS AL	*11
	TOACOR.2,TOMLR.1L	F3	
AECW	TOARIR.2,TOMRK.0L,	AM,AL	*12
	ALIR.2,SF.0H	F1 = F	
AECW2	RDWA=ALIR.1,AR.3,	READ SHSL(1)	*13
	ARIR.2,SF.0L,ROUND,	PASS AM,ROUND AL	*
	TOACOR.0,TOMLR.1H,SETCS	F1,SET STATUS 6	
AECW	MLR.0L,MRR.1H,	AL=A*DL	*14
	ALIR.3C,ACOR.0C,AROR.2TS,SF.0H,	F4=-F1-D+1C	*
	TOMRR.0H	AM	
AECW2	RDWA=MLR.0,ALIR.0,AR.2,AAR,	READ DMHL(3)	*15
	MLR.1L,MRR.0L,ROUND,	3AL=F3*AL,ROUND AM	*
	TOACOR.3,TOMLR.2L	F4	
AECW	MLR.1H,MRR.0H,	1AM=F1*AM	*16
	TOARIR.3,	AL	*
	ALIR.3,ACOR.0,SF.0H	F2=F1+D	
AECW2	RDWA=MLR.3,AR.4,SAR,	DUMMY READ	*17
	TOARIR.0,	3AL	*
	ARIR.3,SF.0L,SETCS,	PASS AL,SET STATUS	*
	TOACOR.1,TOMLR.2H,	F2	*
	RNZ,A	BRANCH TO MIPL0	
AECW	MLR.0H,MRR.1H,	AM=A*DH	*18
	TOACIR.0,TOMRK.0L,	1AM,AL	*

	ALIR,3C,ACOR,1C,AROR,2TS,SF,0H	F3=-F2-D+1C	
AECW2	MLR,2L,MRR,0H,	4AH=F4*AH	*19
	ALIR,1H,ACIR,0,ARIR,0,SF,1H,	0H=SH+1AH+3AL	*
	TOACOR,2,TOMLR,1L,ROUND,	F3,ROUND AL	*
	BCR,1	BRANCH TOI002 ON F2	
OUT PHASE START SEQUENCE			
AECW	SF,0H	NOP	20
AECW2	RDWA=MRR,1,ACIR,1,AR,0,	READ A, -1	*21
	TOALOR,0,SF,0H	0=INHIBIT	
AECW	SF,0H,TOAROR,0	0TO 0C	22
AECW2	RDWA=MLR,0,ALIR,0,AR,2,	READ DHDL(1)	*23
	TOAROR,3	0 TO 1C	
AECW	ALOR,0C,AROH,0C,ACIR,1LC,SF,0H	ONE=-1 -EPS	24
AECW2	RDWA=ALIR,2,AR,1,	READ F	*25
	ALOR,0C,AROR,0C,ACIR,1LC,SF,0H,	ONE=-1 -EPS	*
	TOAROR,1	ONE TO 0C	
AECW	MLR,0H,MRR,1H,	AM=A*DH	*26
	TOAROR,2	ONE TO 1C	
AECW2	RDWA=ALIR,3,AR,1,AAR	READ 0	27
AECW	MLR,0L,MRR,1H,	AL=A*DL	*28
	TOARIR,2,	AM	*
	ALIR,2C,AROR,1,SF,0H	F4=ONE-F	
AECW2	RDWA=MLR,0,ALIR,0,AR,2,AAR,	READ DHDL(2)	*29
	ARIR,2,SF,0L,	PASS AM	*
	TOACOR,3,TOMLR,2L	F4	
AECW	TOARIR,3,TOMRR,0H,	AL,AM	*30
	ALIR,2,SF,0H	F2=F	
AECW2	RDWA=ACIR,3,AR,4,SAR,	DUMMY READ	*31
	ARIR,3,SF,0L,ROUND,	PASS AL,ROUND AM	*
	TOACOR,1,TOMLR,2H,SETCS	F2	
AECW	MLR,0H,MRR,1H,	AM=A*DH	*32
	ALIR,3C,ACOR,1C,AROR,2,SF,0H,	F3=-F2-D+ONE	*
	TOMRR,0L	AL	
AECW2	RDWA=ALIR,1,AR,3,	READ SHSL(1)	*33
	MLR,2L,MRR,0H,ROUND,	4AH=F4*AH,ROUND AL	*
	TOACOR,2,TOMLR,1L	F3	
AECW	MLR,2H,MRR,0L,	2AL=F2*AL	*34
	TOARIR,2,	AM	*
	ALIR,3,ACOR,1,SF,0H	F1=F2+D	
AECW2	RDWA=MLR,0,ALIR,0,AR,2,AAR,	READ DHDL(3)	*35
	TOARIR,1,	4AH	*
	ARIR,2,SF,0L,	PASS AM	*
	TOACOR,0,TOMLR,1H,SETCS,	F1	*
	BNZ,B	BRANCH TO MUPL0	
AECW	MLR,0L,MRR,1H,	AL=A*DL	*36
	TOACIR,1,	2AL	*
	ALIR,3C,ACOR,0C,AROR,2TS,SF,0H,	F4=-D-F1+1C	*
	TOMRR,0H	AM	
AECW2	MLR,1L,MRR,0L,	3AL=F3*AL	*37
	ALIR,1H,ACIR,1,ARIR,1,SF,1H,	0H=SH+2AL+4AH	*
	TOMLR,2L,TOACOR,3,ROUND,	F4,ROUND	*
	BCR,4	BRANCH TO OI01 ON F1	
INPHASE PROCESSING LOOP			
AECW	MLR,0H,MRR,1H,	AM=A*DH	*38
	TOACIR,0,	1AH	*

		ALIR,3C,ACOR,1C,AROR,2TS,SF,0H, TOMPR,0L	F3=-D-F2+1C AL	*
	AECW2	MLR,2L,MRR,0H, ALIR,1H,ACIR,0,ARIR,0,SF,1H, TOACOR,2,TOMLR,1L,ROUND, WRM=AEOR,0,AR,4,AAR, BCR,1	4AH=F4*AH OH=SH+1AH+3AL F3,ROUND AL WRITE OUTPUT OHOL BRANCH ON F2 TO 1002	*39 * * *
MIPL0	AECW	MLR,2H,MRR,0L, TOAIR,2, ALIR,3,ACOR,1,AROR,0TS,SF,0H, TOAFOR,0H	2AL=F2*AL AH F1=D+F2+0C OH	*40 * * *
	AECW2	ROWA=MLR,0,ALIR,0,AR,2,AAR, TOAIR,1,ROUND, ARIR,2,SF,0L, TOACOR,0,TOMLR,1H,SETCS	READ OHOL 4AH,ROUND OH PASS AH F1	*41 * *
MIPL2	AECW	MLR,0L,MRR,1H, TOACIR,1, ALIR,3C,ACOR,0C,AROR,2TS,SF,0H, TOMPR,0H	AL=A*OL 2AL F4=-D-F1+1C AH	*42 * * *
	AECW2	ROWA=ALIR,1,AR,3,AAR, MLR,1L,MRR,0L,ROUND, ALIR,1L,ACIR,1,ARIR,1,SF,1H, TOACOR,3,TOMLR,2L, BNZ,8	READ SHSL 3AL=F3*AL,ROUND AH OL=SL+2AL+4AH F4 BRANCH ON CT TO MIPL	*43 * * *
MIPL1	AECW	MLR,1H,MRR,0H, TOAIR,3, ALIR,3,ACOR,0,AROR,0TS,SF,0H, TOAFOR,0L	1AH=F1*AH AL F2=D+F1+0C OL	*44 * * *
	AECW2	TOAIR,0, ARIR,3,SF,0L,ROUND, TOACOR,1,TOMLR,2H,SETCS, BCR,0	3AL PASS AL,ROUND OL F2 BRANCH ON F1 TO 1001	*45 * *
	AECW	SF,0H	NOP	46
	AECW2	WRM=AEOR,0,AR,4,AAR, BNZ,C	WRITE LAST OUTPUT BRANCH TO STOP	*47
STOP	AECW	SF,0H	NOP	48
	AECW2	STOP	STOP	49
		OUT PHASE PROCESSING LOOP		
MOPLP	AECW	MLR,0L,MRR,1H, TOACIR,1, ALIR,3C,ACOR,0C,AROR,2TS,SF,0H, TOMPR,0H	AL=A*OL 2AL F4=-D-F1+1C AH	*50 * * *
	AECW2	MLR,1L,MRR,0L,ROUND, ALIR,1H,ACIR,1,ARIR,1,SF,1H, TOACOR,3,TOMLR,2L, WRM=AEOR,0,AR,4,AAR, RCR,4	3AL=F3*AL,ROUND AH OH=SH+2AL+4AH F4 WRITE OUTPUT 0 BRANCH TO 0101 ON F1	*51 * * *
MOPL0	AECW	MLR,1H,MRR,0H, TOAIR,3, ALIR,3,ACOR,0,AROR,0S,SF,0H, TOAEOR,0H	1AH=F1*AH AL F2=F1+D+0C OH	*52 * * *
	AECW2	TOAIR,0,ROUND, ARIR,3,SF,0L, TOACOR,1,TOMLR,2H,SETCS	3AL,ROUND OH PASS AL F2	*53 * *
MOPL2	AECW	MLR,0H,MRR,1H, TOACIR,0, ALIR,3C,ACOR,1C,AROR,2TS,SF,0H,	AH=A*OH 1AH F3=-D-F2+1C	*54 * *

		TOMRR.0L	AL	
	AECW2	RDWR=ALIR.1,AM.3,AAR,	READ SHSL	*55
		MLR.2L,MRR.0H,ROUND,	4AH=F4*AH,ROUND AL	*
		ALIR.1L,ACIR.0,ARIR.0,SF.1H,	OL=SL+1AH+3AL	*
		TOACOR.2,TOMLR.1L,	F3	*
		BNZ.9	BRANCH ON CT TO MOPLP	
MOPL1	AECW	MLR.2H,MRR.0L,	2AL=F2*AL	*56
		TOARIR.2,	AM	*
		ALIR.3,ACOR.1,AROR.0TS,SF.0H,	F1=F2+D+0C	*
		TOAFOR.0L	OL	
	AECW2	RDWA=MLR.0,ALIR.0,AR.2,AAR,	READ DHDL	*57
		TOARIR.1,ROUND,	4AH,ROUND OL	*
		ARIR.2,SF.0L,	PASS AM	*
		TOACOR.0,TOMLR.1H,SETCS,	F1	*
		BCR.5	BRANCH TO 0102 ON F2	
	AECW	SF.0H	NOP	58
	AECW2	WRM=AEOR.0,AR.4,AAR,	WRITE LAST OUTPUT	*59
		BNZ.C	BRANCH TO STOP	
	AECW	SF.0H	NOP	60
	AECW2	STOP	STOP	61
		IN TO OUT TRANSITIONS, U POSITIVE		
PI001	AECW	MLR.1H,MRR.0L,	1AL=F1*AL	*62
		TOARIR.2,	AM	*
		ALIR.1H,ARIR.3,SF.1H	OT=SH*AL	
	AECW2	RDWA=MLR.0,ALIR.0,AR.2,AAR,	READ DHDL	*63
		ARIR.2,SF.0L,	PASS AM	*
		TOALOR.0	OT	
	AECW	MLR.0L,MRR.1H,	AL=A*DL	*64
		TOARIR.0,	1AL	*
		ACOR.2,SF.0H,	F4=F3	*
		TOMRR.0H	AM	
	AECW2	MLR.2L,MRR.0L,ROUND,	3AL=F4*AL,ROUND AM	*65
		ALOR.0,ACIR.0C,ARIR.0,SF.1H,	OH=OT-1AH+1AL	*
		TOACOR.3,TOMLR.2L,	F4	*
		BR.7	BRANCH TO MOPL2	
	AECW	MLR.2H,MRR.0H,	1AH=F2*AH	*66
		TOARIR.3,	AL	*
		ALIR.3,ACOR.1,SF.0H,	F2=F2+D	*
		TOAFOR.0H	OH	
	AECW2	TOARIR.0,	3AL	*67
		ARIR.3,SF.0L,ROUND,	PASS AL,ROUND OH	*
		TOACOR.1,TOMLR.2H	F2	
PI002	AECW	MLR.0L,MRR.1H,	AL=A*DL	*69
		TOACIR.1,	2AL	*
		TOMRR.0H	AM	
	AECW2	ACOR.2,SF.0H,ROUND	F4=F3, ROUND AM	69
	AECW	MLR.2L,MRR.0H,	4AH=F4*AH	*70
		TOARIR.3,TOACOR.3,TOMLR.2L,	AL. F4	*
		ACOR.0,SF.0H	F2=F1	
	AECW2	ARIR.3,SF.0L,	PASS AL	*71
		TOACOR.1,TOMLR.2H,	F2	*
		BR.7	BRANCH TO MOPL1	
	AECW	MLR.0H,MRR.1H,	AM=A*OH	*72
		TOARIR.1,	4AH	*
		ALIR.3C,ACOR.1C,AROR.1,SF.0H,	F3=-D-F2+ONE	*
		TOMRR.0L	AL	

	AECW2	RDWR=ALIR.1,AR.3,AAR, MLR.2L,MRR.0H,ROUND, ALIP.1L,ACIR.1C,ARIR.1C,SF.1H, TOACOR.2,TOMLR.1L, BNZ.9	READ SHSL 4AH=F4*AH,ROUND AL OL=SL-2AL-4AH F3 BRANCH ON CT TO MOPLP	*73 * * *
* * * * OUT TO IN TRANSITIONS, D POSITIVE				
POI01	AECW	MLR.0H,MRR.1H, TOACIR.0, TOMRR.0L	AH=A*0H 1AH AL	*74 * *
	AECW2	ACOR.3,SF.0H,ROUND	F3=F4,ROUND AL	75
	AECW	MLR.1L,MRR.0L, TOAIR.2, TOACOR.2,TOMLR.1L, ACOR.1,SF.0H	3AL=F3*AL AH F3 F1=F2	*76 * * *
	AECW2	RDWA=MLR.0,ALIR.0,AR.2,AAR, ARIP.2,SF.0L, TOACOR.0,TOMLR.1H, BR.6	READ DMOL PASS AH F1 BRANCH TO MIPL1	*77 * * *
	AECW	MLR.0L,MRR.1H, TOAIR.0, ALIR.3C,ACOR.0C,AROR.1,SF.0H, TOMRR.0H	AL=A*DL 3AL F4=-D-F1*ONE AH	*78 * * *
	AECW2	RDWR=ALIR.1,AR.3,AAR, MLR.1L,MRR.0L,ROUND, ALIP.1L,ACIR.0C,ARIP.0C,SF.1H, TOACOR.3,TOMLR.2L, BNZ.8	READ SHSL 3AL=F3*AL,ROUND AH OL=SL-1AH-3AL F4 BRANCH ON CT TO MIPLP	*79 * * * *
* * POI02				
	AECW	MLR.2H,MRR.0H, TOAIR.3, ALIR.1H,ARIR.2,SF.1H TOALOR.0,	2AH=F2*AH AL OT=SH+AH OT	*80 * * *81
	AECW2	ARIR.3,SF.0L	PASS AL	
	AECW	MLR.0H,MRR.1H, TOAIR.1, TOMRR.0L, ACOR.3,SF.0H	AH=A*DH 2AH AL F3=F4	*82 * * *
	AECW2	MLR.1L,MRR.0H,ROUND, ALOR.0,ACIR.1C,ARIP.1,SF.1H, TOACOR.2,TOMLR.1L, BR.2	4AH=F3*AH,ROUND AL OH=OT-2AL-2AH F3 BRANCH TO MIPL2	*83 * * *
	AECW	MLR.1H,MRR.0L, TOAIR.2, ALIR.3,ACOR.0,SF.0H, TOAOR.0H	2AL-F1*AL AH F1=F1+D OH	*84 * * *
	AECW2	RDWA=MLR.0,ALIR.0,AR.2,AAR, ARIR.2,SF.0L,ROUND, TOAIR.1,TOACOR.0,TOMLR.1H	READ DMOL ROUND OH, PASS AH F1	*85 * *
* * IN TO OUT TRANSITIONS, D NEGATIVE				
MI001	AECW	ALIP.1H,ARIR.0C,SF.1H	OH=SH-3AL	*86
	AECW2	TOAOR.0H, ALIR.3C,ACOR.1C,AROR.1,SF.0H	OH F4=-D-F2+1 F2=D*F2	*87 * *88
	AECW	ALIR.3,ACOR.1,SF.0H, MLR.2H,MRR.0H, TOMLR.2L,ROUND	1AH=F2*AH F4,ROUND OH	* *

NSWC TR 81-313

	AECW2	ALIR.3,ACOR.1,SF.0H, TOACOR.1, BR.7	F2=D+F2 F2 BRANCH TO MOPL1	*89 *	
	AECW	MLR.0H,MRR.1H, ALIR.3C,ACOR.1C,AROR.1,SF.0H, TOACIR.0, TOMLR.2H	AM=A*DH F3=-D-F2+ONE 1AH F2	*90 * *	
	AECW2	RDWR=ALIR.1,AR.3,AAR, MLR.2L,MRR.0H, ALIR.1L,ACIR.0,SF.1H, TOACOR.2,TOMLR.1L, BNZ.9	READ SHSL 4AH=F4*AH OL=SL+1AH F3 BRANCH ON CT TO MOPLP	*91 * * *	
•	MI002	AECW	SF.0H	NOP	92
	AECW2	RDWR=MLR.0,ALIR.0,AR.2,SAR	BACKUP DMHL AR.2		93
	AECW	ACOR.0,SF.0H	F2=F1		94
	AECW2	TOACOR.1,TOMLR.2H, BR.7	F2 BRANCH TO MOPL1	*95	
	AECW	MLR.0H,MRR.1H, ALIP.3C,ACOR.0C,AROR.1,SF.0H	AM=A*DH F3=-D-F1+ONE	*96	
	AECW2	RDWR=ALIR.1,AR.3,AAR, MLR.1L,MRR.0H, ALIR.1L,ARIR.1C,SF.1H, TOACOR.2,TOMLR.1L, BNZ.9	READ SHSL 4AH=F3*AH OL=SL-4AH F3 BRANCH ON CT TO MOPLP	*97 * * *	
•	•	OUT TO IN TRANSITIONS. D NEGATIVE			
•	MOI01	AECW	SF.0H	NOOP	98
	AECW2	ARIR.3C,SF.0L	DLT=-AL		99
	AECW	TOMLR.3H	DLT		100
	AECW2	ACOR.1,SF.0H, BR.6	F1=F2 BRANCH TO MIPL1	*101	
	AECW	MLR.3H,MRR.1L, ALIP.3C,ACOR.3,SF.0H, TOACOR.0,TOMLR.1H	AL=-1*DLT F4=F4-D F1	*102 * *	
	AECW2	MLR.2L,MRR.0L, ALIR.1L,ACIR.1,ARIR.0C,SF.1H, TOACOR.3,TOMLR.2L, RDWR=ALIR.1,AR.3,AAR, BNZ.8	3AL=F4*AL OL=SL+2AL-3AL F4 READ SHSL BRANCH ON COUNT MIPLP	*103 * * *	
•	MOI02	AECW	TOAIR.3, ALIR.1H,ACIR.0,ARIR.1C,SF.1H	AL OH=SH+1AH-4AH	*104
	AECW2	ARIR.3C,SF.0L, TOAFOR.0H	DLT=-AL OH	*105	
	AECW	MLR.1H,MRR.0L, ALIR.3,ACOR.0,SF.0H, TOMLR.3H,ROUND	1AL=F1*AL F1=F1+D DLT,ROUND OH F1	*106 * *	
	AECW2	TOACOR.0,TOMLR.1H, BR.6	BRANCH TO MIPL1	*107	
	AECW	MLR.3H,MRR.1L, TOAIR.0, ALIR.3C,ACOR.3,SF.0H	AL=DLT*-1 1AL F4=F4-D	*104 * *	
	AECW2	RDWR=ALIR.1,AR.3,AAR, MLR.2L,MRR.0L, ALIR.1L,ACIR.0,ARIR.0,SF.1H, TOACOR.3,TOMLR.2L, BNZ.8	READ SHSL 3AL=F4*AL OL=SL+1AH+1AL F4 BRANCH ON CT TO MIPLP	*109 * * *	

SSSSSSSS	SSSSSSSS	SS	SSSSSSSS	SSSSSSSSSS
SSSSSSSSSS	SSSSSSSSSS	SS	SSSSSSSSSS	SSSSSSSSSS
SS S	SS S	SS	SS SS	SS
SS	SS	SS	SS SS	SS
SSSSSSSS	SS	SS	SS SS	SSS
SSSSSSSS	SS	SS	SSSSSSSS	SSS
SS	SS	SS	SSSSSSSS	SS
S SS	SS S	SS	SS SS	S SS
SSSSSSSS	SSSSSSSS	SSSSSSSS	SS SS	SSSSSSSS
SSSSSS	SSSSSS	SSSSSS	SS SS	SSSSSS

*COMDECK	SCLA3	SF.0H	NOP	0
SCLA3	AECW	RDWH=MRR.0,AR.0	READ A.8	1
	AECW2	SF.0H	NOP	2
	AECW2	RDWH=MRR.1,AR.0,AAR	READ C	3
	AECW	SF.0H	NOP	4
	AECW2	RDWH=MLR.0,AR.1	READ X1,X2	5
	AECW	SF.0H	NOP	6
	AECW2	RDWH=MLR.1,AR.2	READ Y1,Y2	7
	AECW	MLR.0H,MRR.0H	AX1=A*X1	8
	AECW2	RDWH=MLR.2,AR.3,	READ Z1,Z2	*9
		MLR.0L,MRR.0H	AX2=A*X2	
	AECW	MLR.1H,MRR.0L,TOALIR.0	BY1=H*Y1, DES AX1	A
	AECW2	RDWH=ALIR.2,AR.4,SAR,	DUMMY READ	*H
		MLR.1L,MRR.0L,TOALIR.1	BY2=H*Y2, DES AX2	
SC3LP	AFCW	MLR.2H,MRR.1H,TOACIR.0	CZ1=C*Z1, DES BY1	C
	AECW2	RDWH=MLR.0,AR.1,AAR,	READ X3,X4	*D
		MLR.2L,MRR.1H,TOACIR.1	CZ2=C*Z2, DES BY2	
	AECW	TOACIR.0	DES CZ1	E
	AECW2	RDWH=MLR.1,AR.2,AAR,	READ Y3,Y4	*F
		TOACIR.1,SF.0H,	DES CZ2	*
		ALIR.0,ACIR.0,ARIR.0	W1=AX1+BY1+CZ1	
	AECW	MLR.0H,MRR.0H,TOAEOR.0H,	AX3=A*X3, DES W1	*10
		ALIR.1,ACIR.1,ARIR.1,SF.0H	W2=AX2+BY2+CZ2	
	AECW2	RDWH=MLR.2,AR.3,AAR,ROUND,	READ Z3,Z4,ROUND W1	*11
		MLR.0L,MRR.0H,	AX4=A*X4	*
		SF.0H,TOAEOR.0L,BN7.9	DES W2, LOOP	
	AECW	MLR.1H,MRR.0L,TOALIR.0,	BY3=H*Y3, DES AX3	*12
		ROUND	ROUND W2	
	AECW2	WRM=AEOR.0,AR.4,AAR,	WRITE W1,W2	*13
		MLR.1L,MRR.0L,TOALIR.1	BY4=H*Y4, DES AX4	
	AECW	SF.0H	NOP	14
	AECW2	STOP	STOP	15


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*COMDECK F22S3
F22S3

AECW	SF.0H	NOP	0
AECW2	RDWR=MRR.2.AR.5	READ FH.FL	1
AECW	SF.0H	NOP	2
AECW2	RDWR=MRR.3.AR.5.AAR	READ GH.GL	3
AECW	SF.0H	NOP	4
AECW2	RDWR=MLR.2.AR.1	READ A.C	5
AECW	SF.0H	NOP	6
AECW2	RDWR=MLR.3.AR.1.AAR	READ H.D	7
AECW	MLR.2H.MRR.2L	AFL=A*FL	H
AECW2	RDWR=MRR.0.AR.1.AAR.	HEAD U.V	*9
	MLR.2L.MRR.3L	CGL=C*GL	
AECW	MLR.3H.MRR.2H.TOACIR.2	HFH=H*FH. DES AFL	A
AECW2	RDWR=MLR.0.AR.2.	HEAD XM.XL	*B
	MLR.3L.MRR.3H.TOACIR.3	DGH=D*GH. DES CGL	
AECW	TOAIR.2	DES BFH	C
AECW2	RDWR=MLR.1.AR.3.	READ YH.YL	*D
	TOAIR.3	DES DGH	
AECW	MLR.0H.MRR.0H	UXH=U*XH	E
AECW2	RDWR=ALIR.1.AR.5.AAR	READ SSH.SSL	F
AECW	MLR.1H.MRR.0L.TOALIR.2	VYH=V*YH. DES UXH	10
AECW2	RDWR=ALIR.0.AP.0.	READ SH.SL	*11
	ALIR.2.ACIR.2.AIR.2.SF.0L	FH=UXH+AFL+BFH	
AECW	MLR.3H.MRR.2L.TOALIR.3.	BFL=B*FL. DES VYH	*12
	ALIR.1L.SF.0H.	PASS SSL	*
	TOACOR.1.TOMRR.2H	DES FH	
AECW2	RDWR=ACIR.0.AR.4.SAR.	DUMMY READ ON OUTPUT	*13
	MLR.3L.MRR.3L.	DGL=D*GL	*
	TOAROR.0.ROUND	DES SSL. RND FH	
AECW	MLR.0L.MRR.0H.TOAHIR.2.	UXL=U*XL. DES BFL	*14
	ALIR.3.ACIR.3.AIR.3.SF.0L.	GH=VYH+CGL+DGH	*
	ROUND	ROUND SSL	
AECW2	RDWR=MLR.0.AR.2.AAR.	READ XM.XL	*15
	MLR.1L.MRR.0L.TOALIR.3.	VYL=V*YL. DES DGL	*
	ACOR.1.SF.0H.	FHO=FM	*
	TOAROR.1.TOMRR.3H	DES GH	
F22LP AECW	MLR.2H.MRR.2H.TOALIR.2.	AFH=A*FH. DES UXL	*16
	ALIR.0H.ACOR.1.AROR.1.SF.0H.	SSH=SH+FH+GH	*
	TOAEOR.1H.ROUND	DES FHO. RND GH	
AECW2	RDWR=MLR.1.AR.3.AAR.	HEAD YH.YL	*17
	MLR.2L.MRR.3H.TOALIR.3.	CGH=C*GH. DES VYL	*
	AROR.1.SF.0H.	GHO=GH	*
	TOACOR.0.ROUND	DES SSH. RND FHO	
AECW	MLR.3H.MRR.2H.TOACIR.2.	BFH=B*FH. DES AFH	*18
	ACOR.0.AROR.0C.SF.1H.	SHO=SSH(-SSL)	*

AECW2	TOAEOR.2H,ROUND	DES GHO, RND SSH	
	MLR.3L,MRR.3H,TOACIR.3.	DGY=D*GH, DES CGH	*19
	ALIR.2,ACIR.2,ARIR.2,SF.0L.	FL=UXL*AFH*HFL	*
	TOAEOR.0H,ROUND	DES SHO, RND GHO	
AECW	MLR.0H,MRR.0H,TOARIR.2.	UXH=U*XH, DES BFM	*1A
	ALIR.3,ACIR.3,ARIR.3,SF.0L.	GL=VYL*CGH*DGL	*
	TOACOR.2,TOMRR.2L,ROUND	UES FL, RND SHO	
AECW2	MLR.1H,MRR.0L,TOARIR.3.	VYH=V*YH, DES DGH	*1B
	ACOR.2,SF.0H.	FLO=FL	*
	TOAROR.2,TOMRR.3L,ROUND	DES GL, RND FL	
AECW	MLR.2H,MRR.2L,TOALIR.2.	AFL=A*FL, DES UXH	*1C
	ALIR.0L,ACOR.2,AROR.2,SF.0H.	SSL=SL*FL*GL	*
	TOAEOR.1L,ROUND	DES FLO, RND GL	
AECW2	RDR=ALIR.0,AR.0,AAR.	READ SH,SL	*1D
	MLR.2L,MRR.3L,TOALIR.3.	CGL=C*GL, DES VYM	*
	AROR.2,SF.0H.	GLO=GL	*
	TOAROR.0,ROUND	DES SSL, RND FLO	
AECW	MLR.3H,MRR.2L,TOACIR.2.	HFL=H*FL, DES AFL	*1E
	AROR.0,ACOR.0C,SF.1L.	SLO=SSL*(-SSH)	*
	TOAEOR.2L,ROUND	DES GLO, RND SSL	
AECW2	RDR=MLR.0,AR.2,AAR.	READ XM,XL	*1F
	MLR.3L,MRR.3L,TOACIR.3.	DGL=U*GL, DES CGL	*
	ALIR.2,ACIR.2,ARIR.2,SF.0L.	FH=UXH*AFL*BFH	*
	TOAEOR.0L,ROUND,BNZ.8	DES SLO, RND GLO, HR	
AECW	MLR.0L,MRR.0H,TOARIR.2.	UXL=U*XL, DES RFL	*20
	ALIR.3,ACIR.3,ARIR.3,SF.0L.	GH=VYM*CGL*DGH	*
	TOACOR.1,TOMRR.2H,ROUND	UES FH, RND SLO	
AECW2	WRM=AEOR.0,AR.4,AAR.	WRITE SHO,SLU	*21
	MLR.1L,MRR.0L,TOARIR.3.	VYL=V*YL, DES DGL	*
	ACOR.1,SF.0H.	FHO=FH	*
	TOAROR.1,TOMRR.3H,ROUND	DES GH, RND FH	
AECW	AROR.0,SF.0H	PASS SSL	22
AECW2	TOAEOR.3L	DES SSL	23
AECW	SF.0H	NOP	24
AECW2	WRM=AEOR.3,AR.5	WRITE SSO	25
AECW	SF.0H	NOP	26
AECW2	WRM=AEOR.2,AR.5,SAR	WRITE GO	27
AECW	SF.0H	NOP	28
AECW2	WRM=AEOR.1,AR.5,SAR	WRITE FO	29
AECW	SF.0H	NOP	2A
AECW2	STOP	STOP	2B

NSWC TR 81-313

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AECW	SF.0H	NOP	0
AECW2	RDWR=ALIR.2.AR.6	READ L1,T1	1
AECW	SF.0H	NOP	2
AECW2	RDWR=MLR.0.AR.6.AAR	HEAD K1,A1	3
AECW	ALIR.2L,SF.1L	PASS T1	4
AECW2	RDWR=MRR.1.AR.6.AAR.TOACOR.0	HEAD H,C. DES T1	5
AECW	SF.0H	NOP	6
AECW2	RDWR=ALIR.3.AR.6.AAR	READ L2,T2	7
AECW	SF.0H	NOP	8
AECW2	RDWR=MRR.2.AR.4.	READ X11,X12	*9
	SCMR.0H=AR.0	COS (S11) AE0	
AECW	ALIR.3L,SF.1L	PASS T2	A
AECW2	RDWR=MLR.2.AR.7.TOACOR.1.	READ Y11,Y12. DES T2	*B
	SCMR.0H=AR.2	COS (S11) AE1	
AECW	SF.0H	NOP	C
AECW2	RDWR=MLR.1.AR.6.AAR	READ K2,A2	D
AECW	SF.0H	NOP	F
AECW2	RDWR=MRR.3.AR.4.AAR.	READ X21,X22	*F
	SCMR.0H=AR.1.	COS (S21) AE0	*
	MLR.0L,MRR.2H	AX11=A1*X11	
AECW	MLR.2H,MRR.1L	CY11=C*Y11	10
AECW2	RDWR=MLR.3.AR.7.AAR.	READ Y21,Y22	*11
	SCMR.0H=AR.3.	COS (S21) AE1	*
	MLR.2L,MRR.1H.TOARIR.0	RY12=R*Y12. DES AX11	
AECW	MLR.0H,MRR.0H.TOACIR.0	KS11=K1*S11. DES CY11	12
AECW2	TOALIR.0	DES BY12	13
AECW	TOAPIR.2	DES KS11	14
AECW2	RDWR=ALIR.1.AR.5.	READ TG1,TG2	*15
	SCMR.0H=AR.0INC.	COS (S12) AE0	*
	MLR.3H,MRR.1L	CY21=C*Y21	
AECW	MLR.1H,MRR.0H.	KS21=K2*S21	*16
	ALIR.2H,ACOR.0C,ARIR.2.SF.1H	P11=L1-T1*KS11	
AECW2	RDWR=ACIR.3.AR.5.SAR.	DUMMY READ ON OUTPUT	*17
	SCMR.0H=AR.2INC.	COS (S12) AE1	*
	MLR.3L,MRR.1H.TOACIR.1.	BY22=B*Y22. DES CY21	*
	ALIR.0.ACIR.0.ARIR.0.SF.0L.	Y11=RY12*CY11*AX11	*
	TOAPOR.0.SETCS	DES P11	
AECW	MLR.1L,MRR.3H.TOARIR.2.	AX21=A2*X21. DES KS21	*18
	ACOR.0.AHOR.0TS.SF.1L.	DM11=T1*(P11)C	*
	TOALOR.0.TOMLR.2H	DES Y11	
AECW2	SCMR.0H=AR.1INC.	COS (S22) AE0	*19
	MLR.2L,MRR.1L.TOALIR.0.	CY12=C*Y12. DES BY22	*
	TOMRR.0L.FOUND	DES DM11. RND Y11	
AECW	MLR.3L,MRR.1L.TOARIR.1.	CY22=C*Y22. DES AX21	*1A

NSWC TR 81-313

AECW2	ALIR.3H.ACOR.1C,ARIR.2,SF.1H SCMR.0H=AR.3INC, MLR.2H,MRR.0L,TOACIR.0, ALIR.0,ACIR.1,ARIR.1,SF.0L, TOAROR.0,SETCS	P21=L2-T2*KS21 COS (S22) AE1 *1H D11=DM11*Y11,DES CY12 * Y21=BY22*CY21*AX21 * DFS P21 KS12=K1*S12, DES CY22 *1C DM21=T2*(P21)C * DES Y21 RY11=H*Y11, DES D11 *1D PAS Y11 * DES DM21, RND Y21 AX12=A1*X12, DES KS12 *1E DES Y11 READ X11,X12 *1F COS (S11) AE0 * D21=DM21*Y21,DES BY11 * P12=L1-T1*KS12 KS22=K2*S22, DES AX12 *20 PASS Y21, DES P12 COS (S11) AE1 *21 RY21=H*Y21, DES D21 * Y12=BY11*CY12*AX12 * DFS Y21 AX22=A2*X22, DES KS22 *22 DM12=T1*(P12)C * DES Y12 COS (S21) AE0 *23 CY11=C*Y11, DES BY21 * P22=L2-T2*KS22 * DES DM12, RND Y12 CY21=C*Y21, DES AX22 *24 TG1=TG1*D11*U21 * DFS P22 COS (S21) AE1 *25 D12=DM12*Y12,DES CY11 * Y22=RY21*CY22*AX22 * DES TG1 KS11=K1*S11, DES CY21 *26 DM22=T2*(P22)C * DES Y22, RND TG1 RY12=H*Y12, DES D12 *27 PASS Y12 * DES DM22, RND Y22 AX11=A1*X11, DES KS11 *29 DES Y12 READ X21,X22 *29 COS (S12) AE0 * U22=UM22*Y22,DES BY12 * P11=L1-T1*KS11 KS21=K2*S21, DES AX11 *2A PASS Y22, DES P11 COS (S12) AE1 *2B RY22=H*Y22, DES D22 * Y11=BY12*CY11*AX11 * DES Y22 AX21=A2*X21, DES KS21 *2C DM11=T1*(P11)C * DES Y11
AECW	MLR.0H,MRR.0H,TOACIR.1, ACOR.1,AROR.0TS,SF.1L, TOALOR.1,TOMLR.3H	
AECW2	MLR.2H,MRR.1H,TOACIR.2, ALOR.0,SF.0H, TOMRR.0L,ROUND	
OMNLP AECW	MLR.0L,MRR.2L,TOARIR.2, TOAENR.0H	
AECW2	RDWR=MRR.2,AR.4,AAR, SCMR.0H=AR.0INC, MLR.3H,MRR.0L,TOALIR.0, ALIR.2H,ACOR.0C,ARIR.2,SF.1H	
AECW	MLR.1H,MRR.0H,TOARIR.0, ALOR.1,SF.0H,TOAROR.0,SETCS	
AECW2	SCMR.0H=AR.2INC, MLR.3H,MRR.1H,TOARIR.3, ALIR.0,ACIR.0,ARIR.0,SF.0L, TOAFOR.1H	
AECW	MLR.1L,MRR.3L,TOARIR.2, ACOR.0,AROR.0TS,SF.1L, TOALOR.2,TOMLR.2L	
AECW2	SCMR.0H=AR.1INC, MLR.2H,MRR.1L,TOALIR.0, ALIR.3H,ACOR.1C,ARIR.2,SF.1H, TOMRR.0L,ROUND	
AECW	MLR.3H,MRR.1L,TOARIR.1, ALIR.1H,ACIR.2,ARIR.3,SF.2H, TOAROR.0,SETCS	
AECW2	SCMR.0H=AR.3INC, MLR.2L,MRR.0L,TOACIR.0, ALIR.0,ACIR.1,ARIR.1,SF.0L, TOAFOR.2H	
AECW	MLR.0H,MRR.0H,TOACIR.1, ACOR.1,AROR.0TS,SF.1L, TOALOR.3,TOMLR.3L,ROUND	
AECW2	MLR.2L,MRR.1H,TOACIR.2, ALOR.2,SF.0H, TOMRR.0L,ROUND	
AECW	MLR.0L,MRR.2H,TOARIR.2, TOAENR.0L	
AECW2	RDWR=MRR.3,AR.4,AAR, SCMR.0H=AR.0INC, MLR.3L,MRR.0L,TOALIR.0, ALIR.2H,ACOR.0C,ARIR.2,SF.1H	
AECW	MLR.1H,MRR.0H,TOARIR.0, ALOR.3,SF.0H,TOAROR.0,SETCS	
AECW2	SCMR.0H=AR.2INC, MLR.2L,MRR.1H,TOARIR.3, ALIR.0,ACIR.0,ARIR.0,SF.0L, TOAFOR.1L	
AECW	MLR.1L,MRR.3H,TOARIR.2, ACOR.0,AROR.0TS,SF.1L, TOALOR.0,TOMLR.2H	

AECW2	PDWR=ALIR.1,AR.5,AIRU.	READ TG1,TG2	*2D
	SCMP.0H=AR.1INC,	COS (S22) AE0	*
	MLR.2L,MHR.1L,TOALIR.0.	CY12=C*Y12, DES BY22	*
	ALIR.3H,ACOR.1C,ARIR.2,SF.1H.	P21=L2-T2+KS21	*
	TOMRP.0L,ROUND	DES DM11, RND Y11	
AECW	MLR.3L,MHR.1L,TOARIR.1.	CY22=C*Y22, DES AX21	*2E
	ALIR.1L,ACIR.2,ARIR.3,SF.2H.	TG2=TG2+D12+U22	*
	TOAROH.0,SETCS	DES P21	
AECW2	SCMP.0H=AR.3INC,	COS (S22) AE1	*2F
	MLR.2H,MHR.0L,TOACIR.0,	U11=DM11*Y11, DES CY12*	
	ALIP.0,ACIR.1,ARIR.1,SF.0L.	Y21=BY22+CY21+AX21	*
	TOAFOR.2L,BNZ.F	DES TG2, BR TO DMNLP	
AECW	MLR.0H,MHR.0H,TOACIR.1,	KS12=K1*S12, DES CY22	*30
	ACOP.1,AROR.0TS,SF.1L.	DM21=T2+(P21)C	*
	TOALOR.1,TOMLN.3H,ROUND	DES Y21, RND TG2	
AECW2	WRM=AEOR.2,AR.5,SAR.	WRITE TG1,TG2	*31
	MLR.2H,MHR.1H,TOACIR.2,	RY11=H*Y11, DES D11	*
	ALOR.0,SF.0H.	PASS Y11	*
	TOMRP.0L,ROUND	UES DM21, RND Y21	
AECW	SF.0H	NOP	32
AECW2	WRM=AEOR.0,AR.7,SAR	WRITE STATES Y11,Y12	33
AECW	SF.0H	NOP	34
AECW2	WRM=AEOR.1,AR.7,AAH	WRITE STATES Y21,Y22	35
AECW	SF.0H	NOP	36
AECW2	STOP	STOP	37

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